IBM Customer Engineering

Instructional Logic Diagrams

1410 Data Processing System

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1410 Data Processing System

This book is designed primarily for instruction purposes. It shows the major logic of the 1410 system, but does not contain all the circuits shown in the ALD's. The ILD's were drawn from second levels contained in existing manuals of instruction and from ALD's with an EC number of 253259. There will be no revision to this manual.

The ILD's are organized throughout CPU by functional unit while the I/O areas are shown by sequence of operation.

All ILD's that have a figure number with the suffix A or B are functional "big pictures" which show the individual Data and Control ILD's for specific functional units.

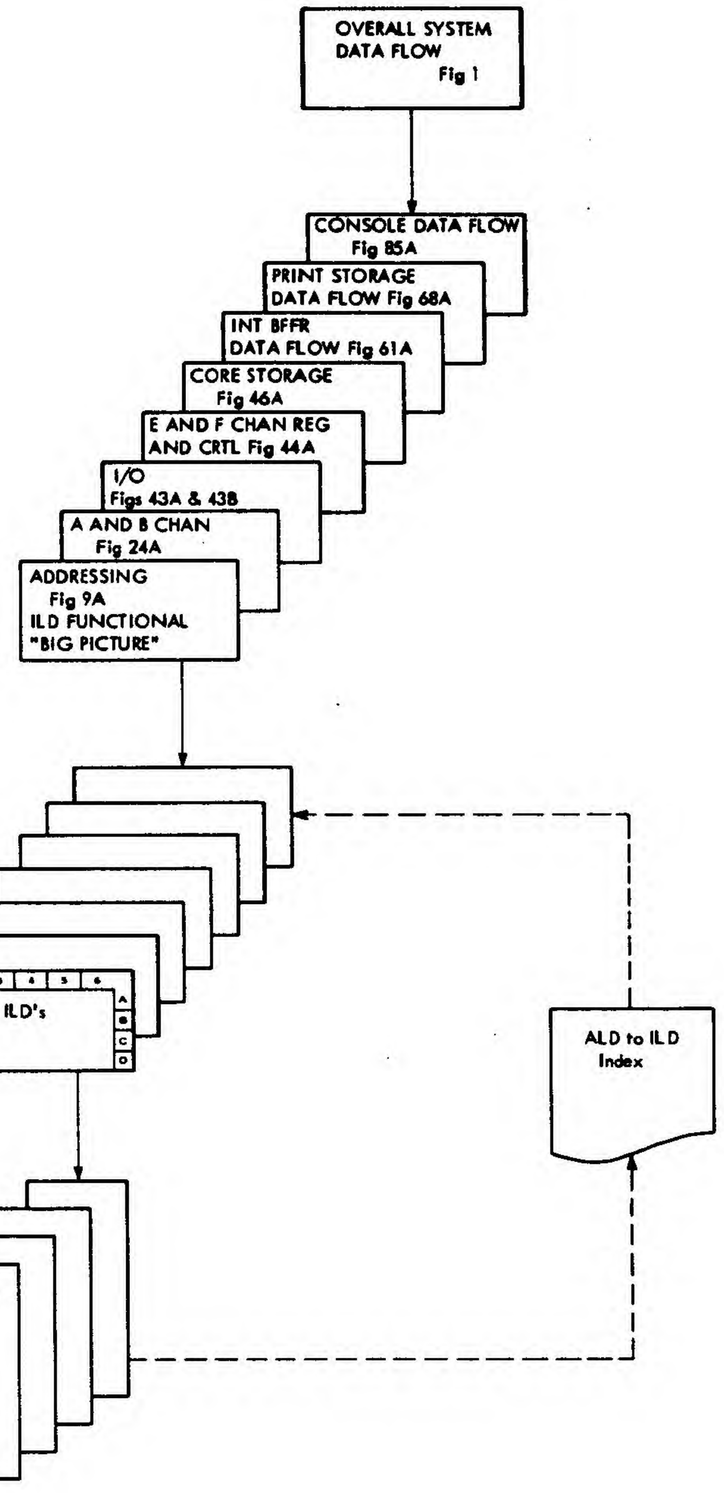
The normal usage path would be from Overall Data Flow to functional "big picture" then to the individual ILD and ultimately to the ALD.

An ALD/ILD Index follows the ILD's. It is arranged in numerical sequence by ALD page number to aid in returning to the ILD's from the ALD's. ILD lines are referenced using a co-ordinate system as follows:

25 D 2

The first number (25) represents the ILD figure number from which or to which the line is referenced. The alphabetic character (D) represents the vertical position on the figure while the last number (2) represents the horizontal position.

The ILD output lines are indexed to the ILD page on which they appear in a listing found after the ILD/ALD index.



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IBM Corporation, Customer Engineering Education, Dept. 911, Poughkeepsie, New York 12602

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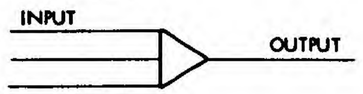
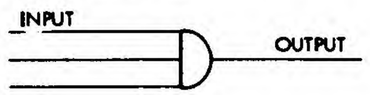
SYMBOLOGY USED THROUGHOUT — 1410 INTERMEDIATE LOGIC DIAGRAMS

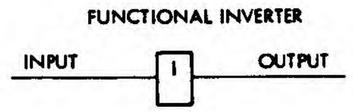
AND CIRCUIT

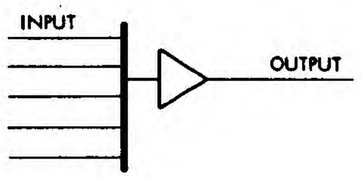


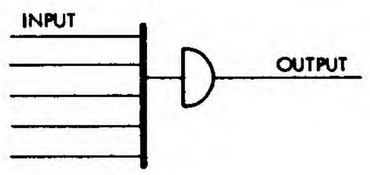
OR CIRCUIT



FUNCTIONAL INVERTER







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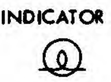
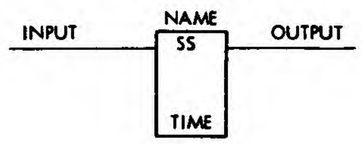
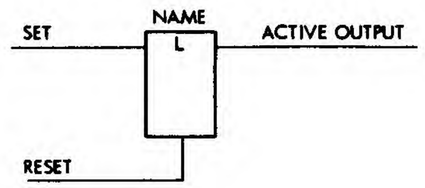
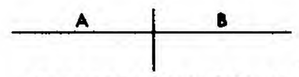


SINGLE SHOT



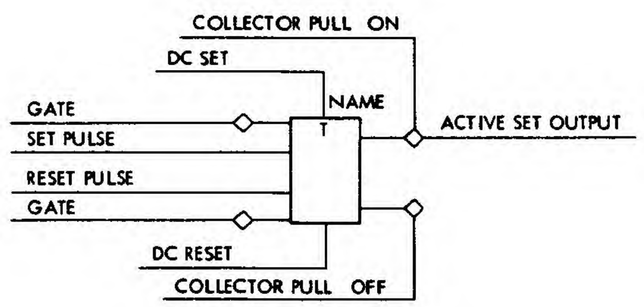
LATCH



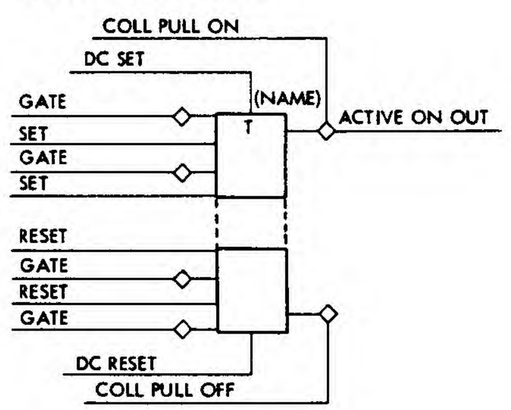


CHANGE LINE NAME ONLY

TRIGGER



DOUBLE SET/RESET TRIGGER



NOTES:

ALL NAMES ENCLOSED IN PARENTHESES ARE FOR LOGICAL EXPLANATION AND DO NOT NECESSARILY APPEAR IN THE ALD'S

ANY ASTERISKS SHOWN ARE AN ACTUAL PART OF THE ALD LINE NAME

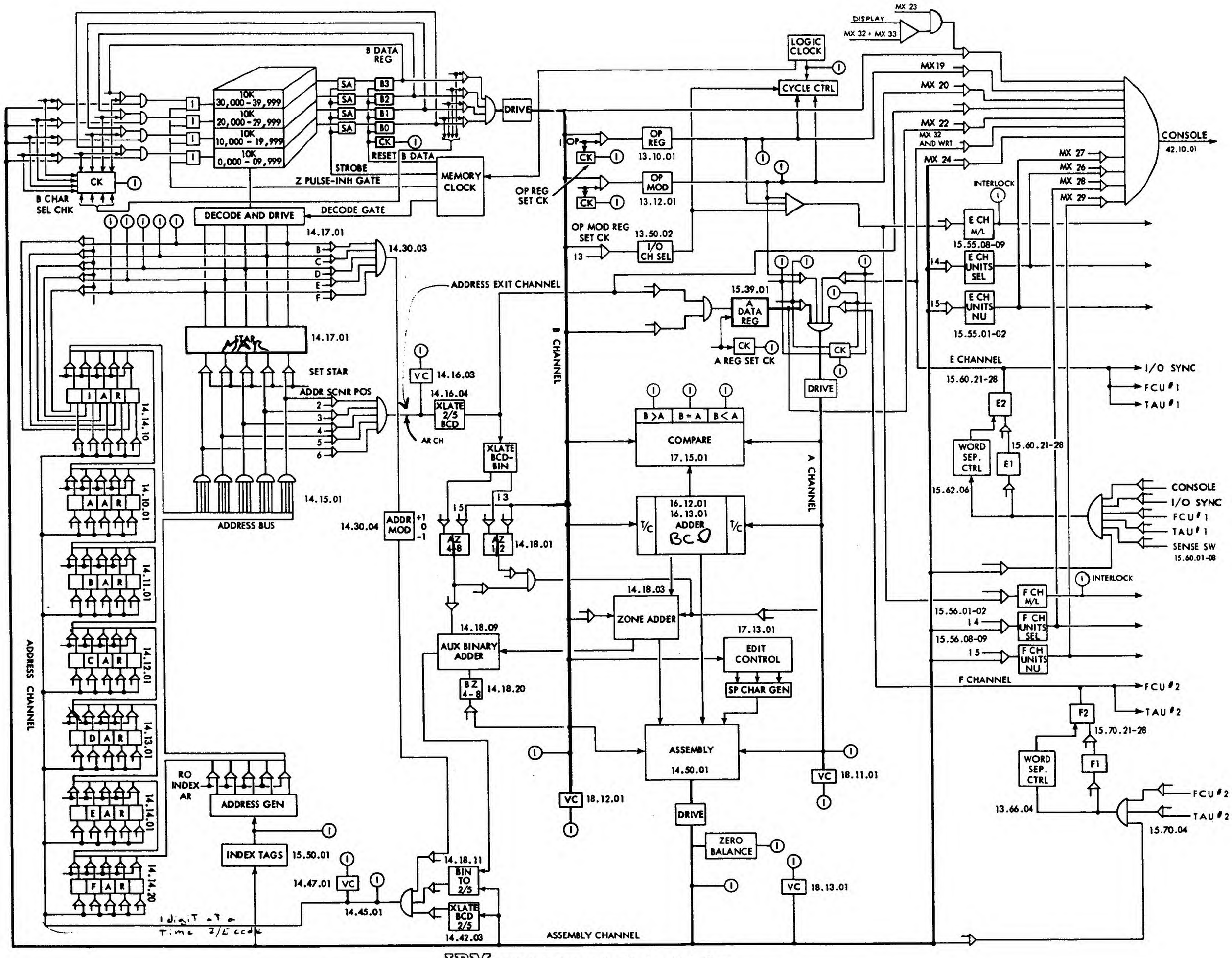
ALL CONDENSED LOGIC DIAGRAMS ARE POSITIVE LOGIC THROUGHOUT

$x > y$

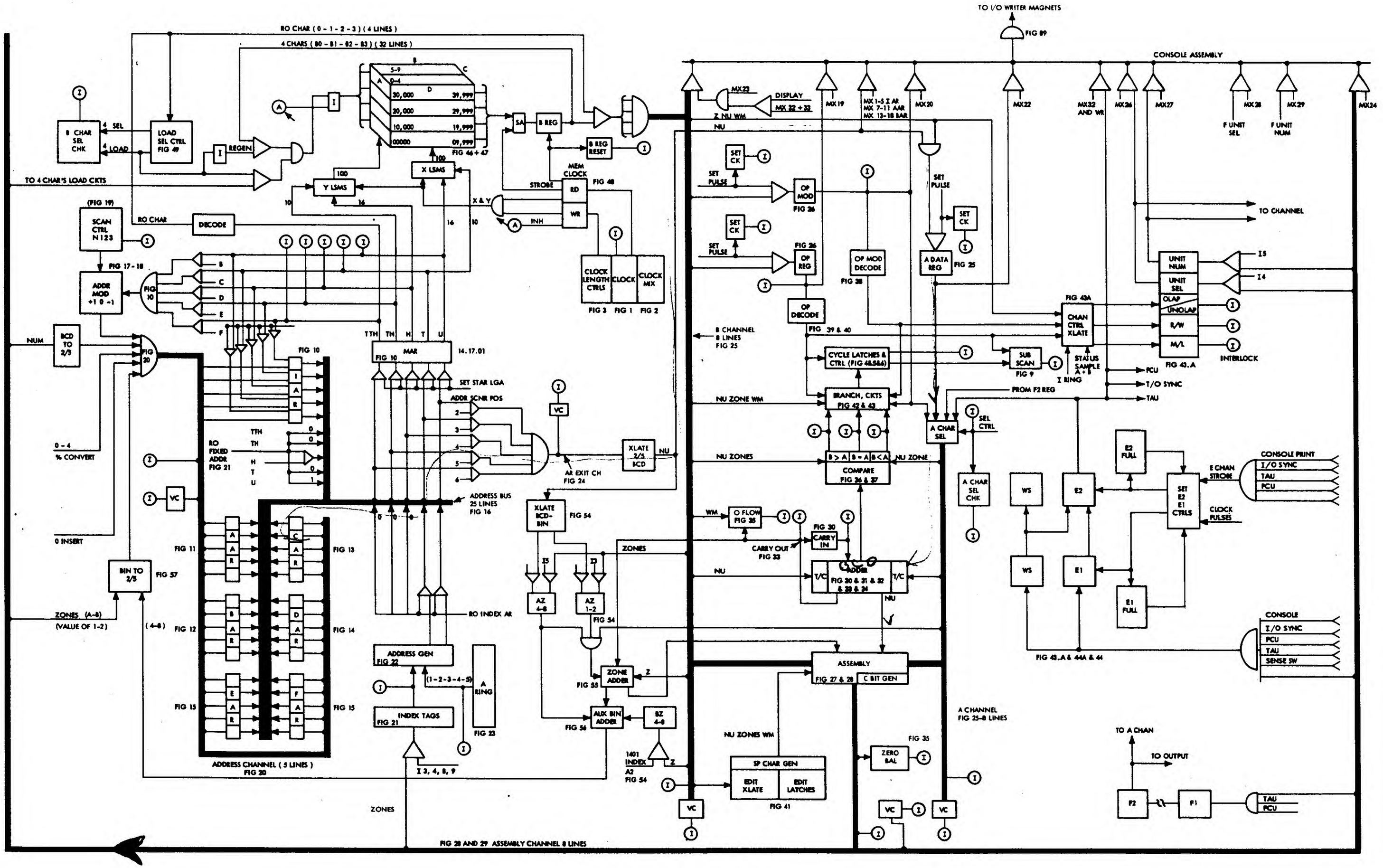
$x < y$

$B > A$ — B greater Than A

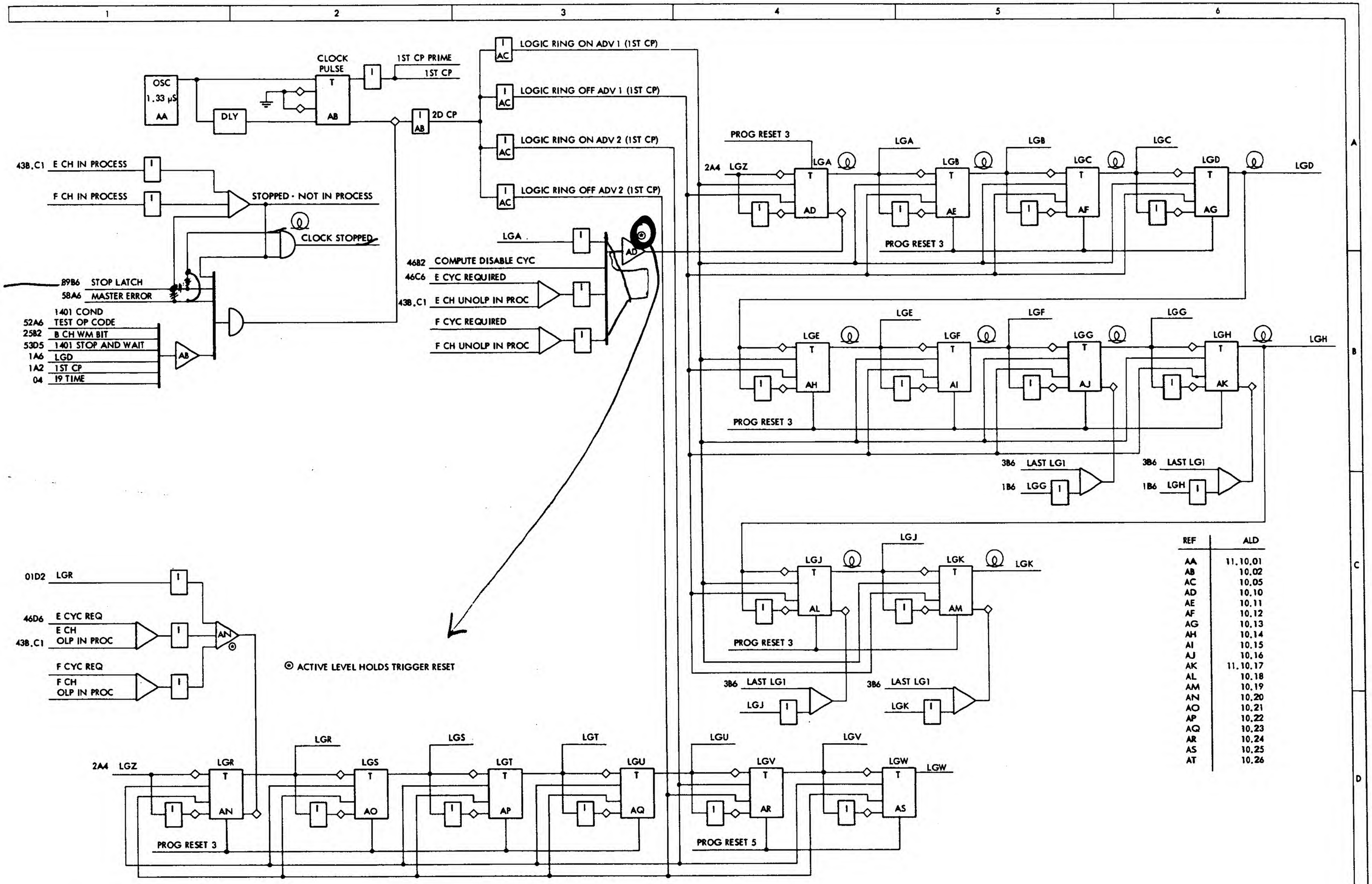
$B < A$ — B Less Than A



IBM 1410 Data Processing System Data Flow



1410 PROCESSING DATA FLOW
(ILD REFERENCE)



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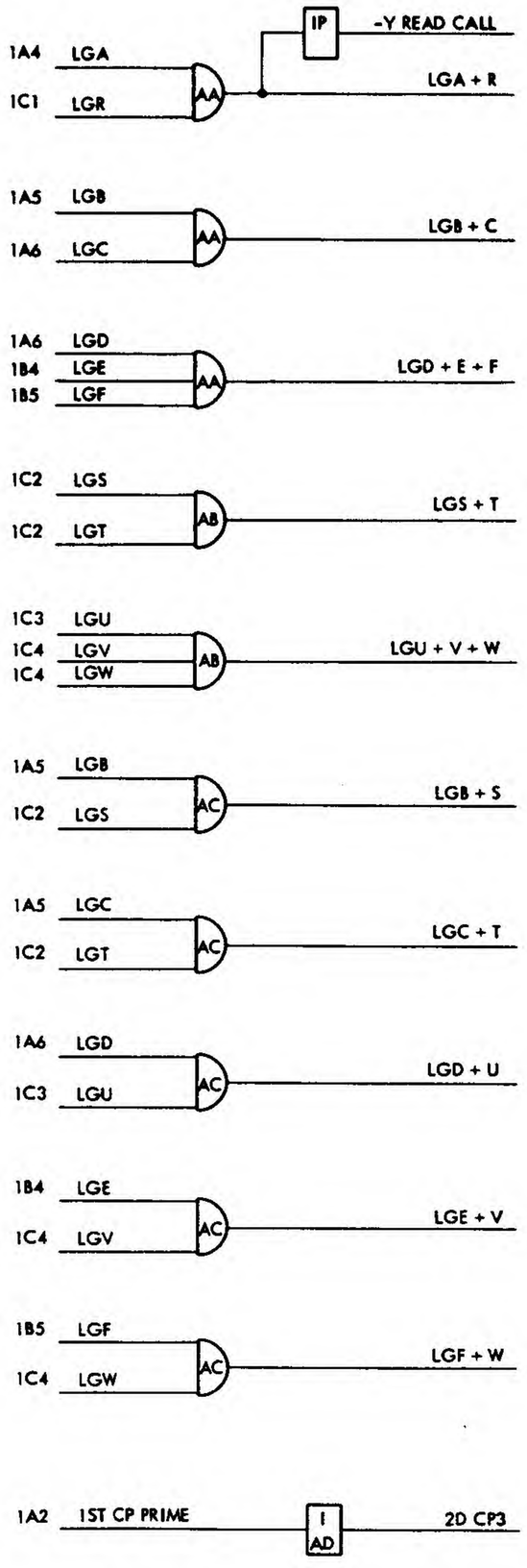
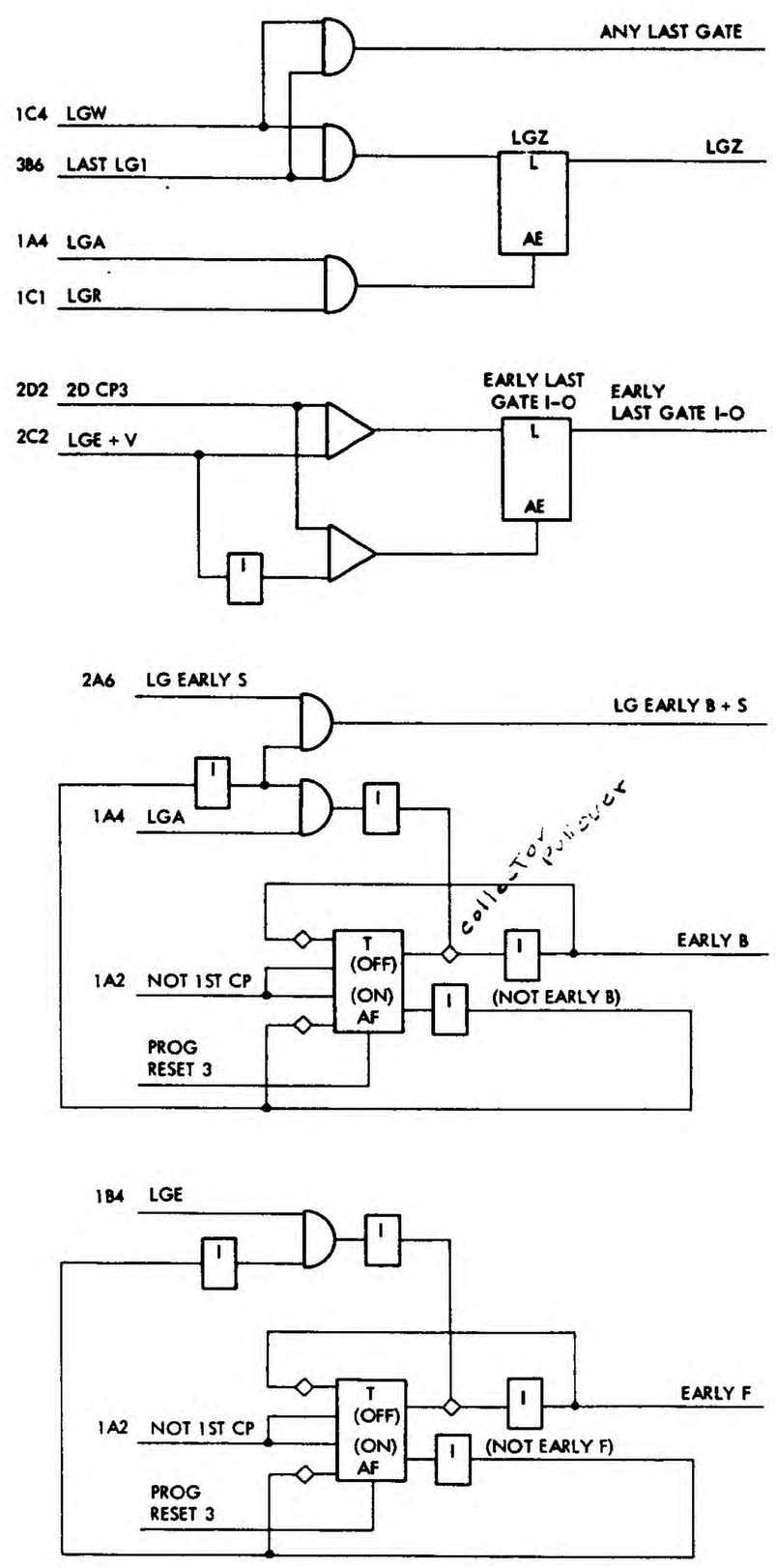
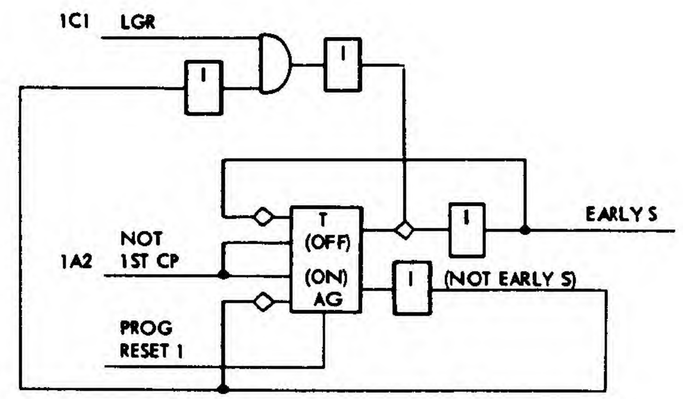
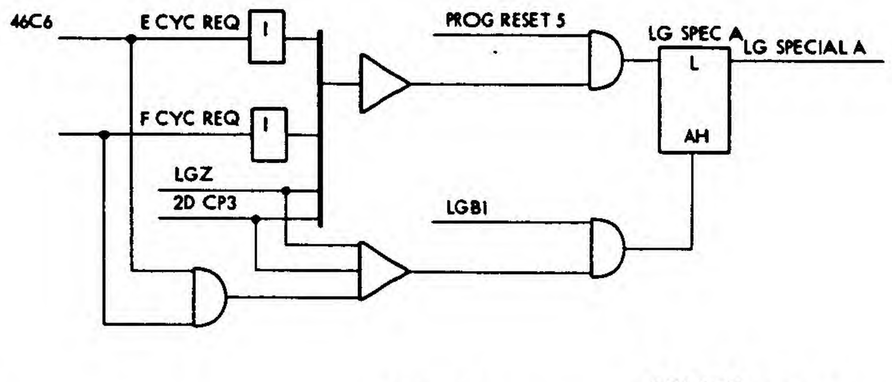
AB	10.02
AC	10.05
AD	10.10
AE	10.11
AF	10.12
AG	10.13
AH	10.14
AI	10.15
AJ	10.16
AK	11.10.17
AL	10.18
AM	10.19
AN	10.20
AO	10.21
AP	10.22
AQ	10.23
AR	10.24
AS	10.25
AT	10.26

FIGURE 1. CLOCK, LOGIC RING, AND LOGIC RING EXTENSION









REF	ALD
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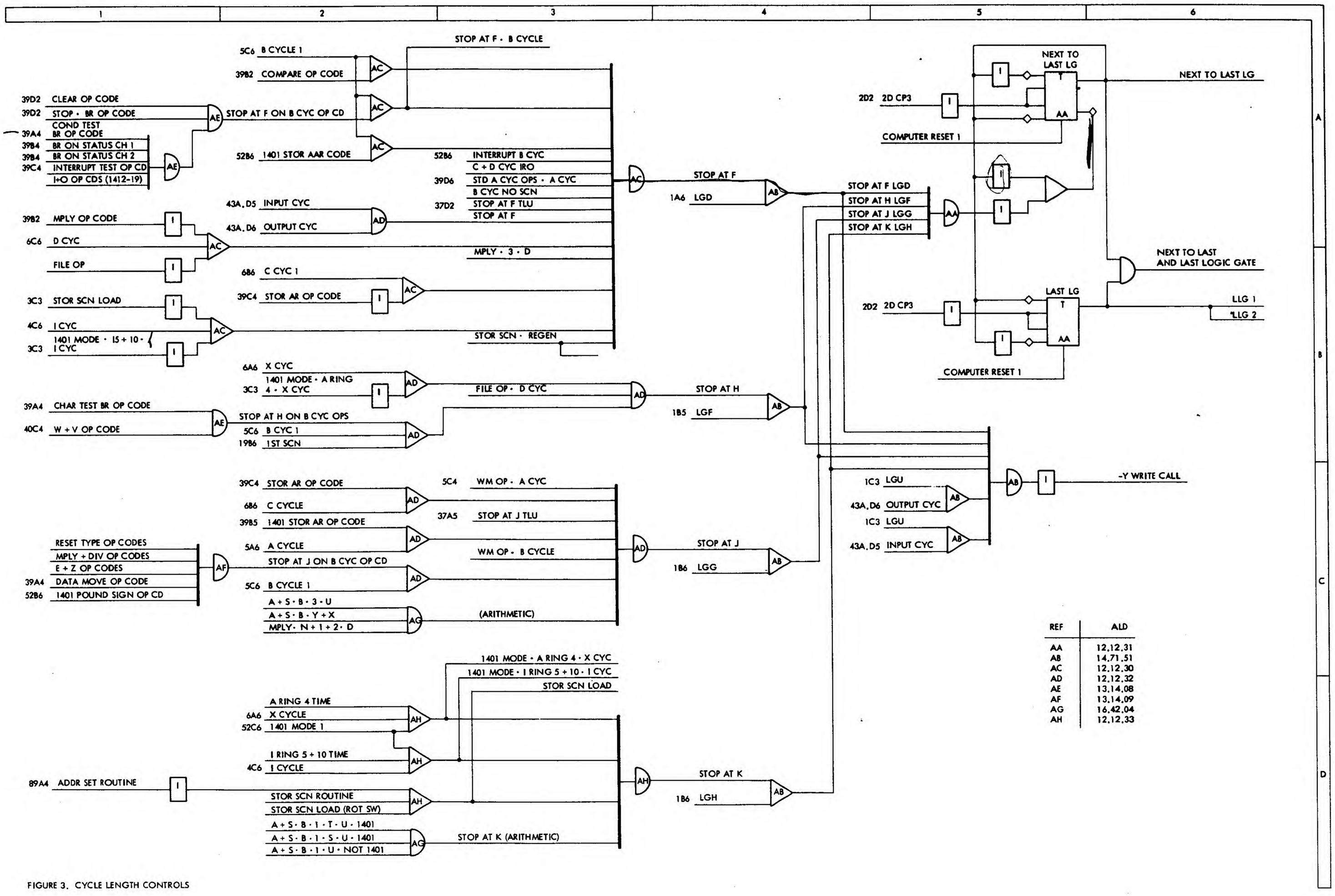
AB	10,33
AC	10,34
AD	10,36
AE	10,06
AF	30.01
AG	30,03
AH	30,02

NOTE: ALL PARENTHESISED NAMES ARE FOR REFERENCE PURPOSES ONLY

FIGURE 2. LOGIC GATE MIX AND SPECIAL LOGIC GATES



REF	ALD
AA	12,12,31
AB	14,71,51
AC	12,12,30
AD	12,12,32
AE	13,14,08
AF	13,14,09
AG	16,42,04
AH	12,12,33

FIGURE 3. CYCLE LENGTH CONTROLS

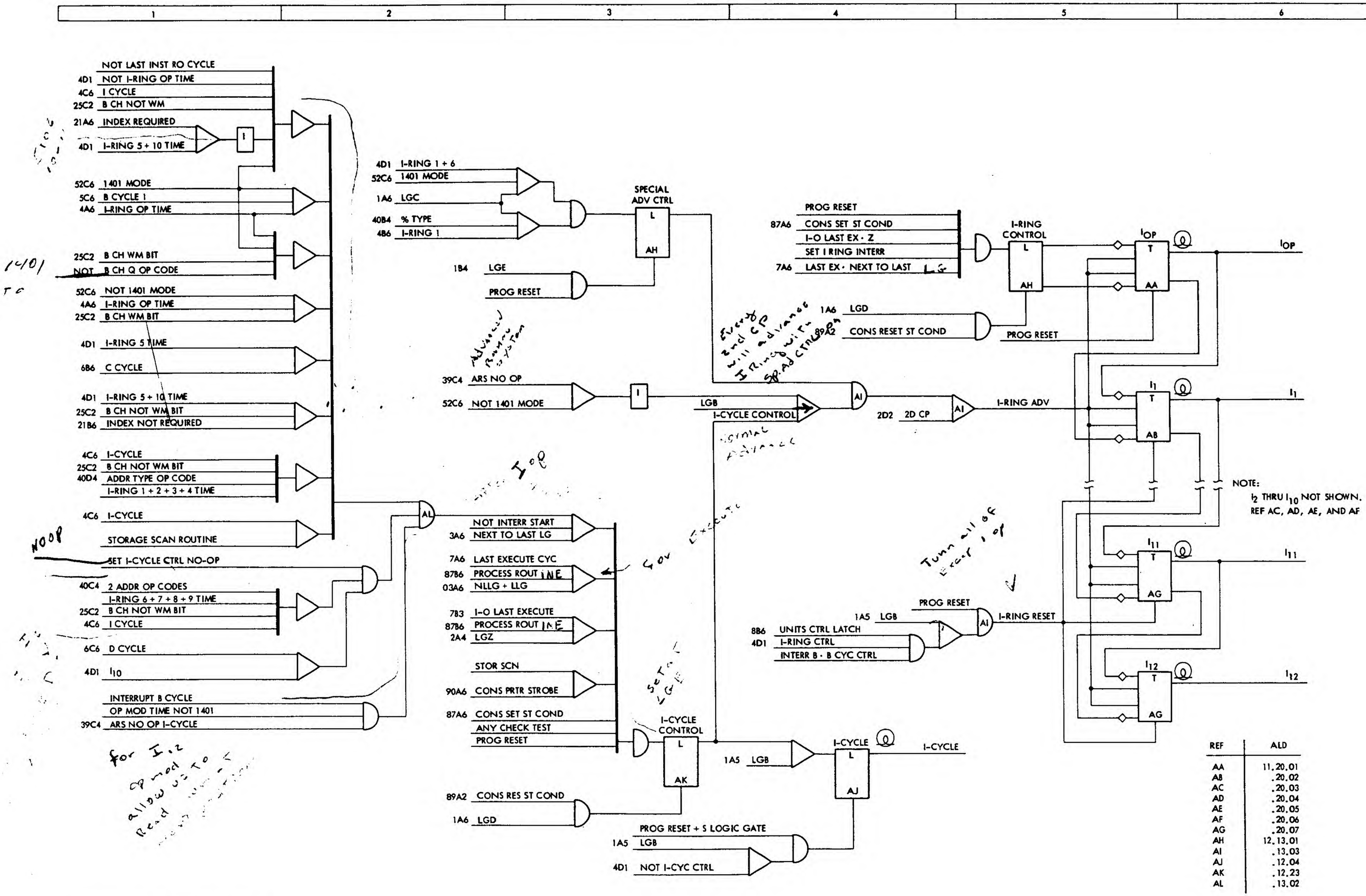


FIGURE 4. I CYCLE CONTROL AND I RING

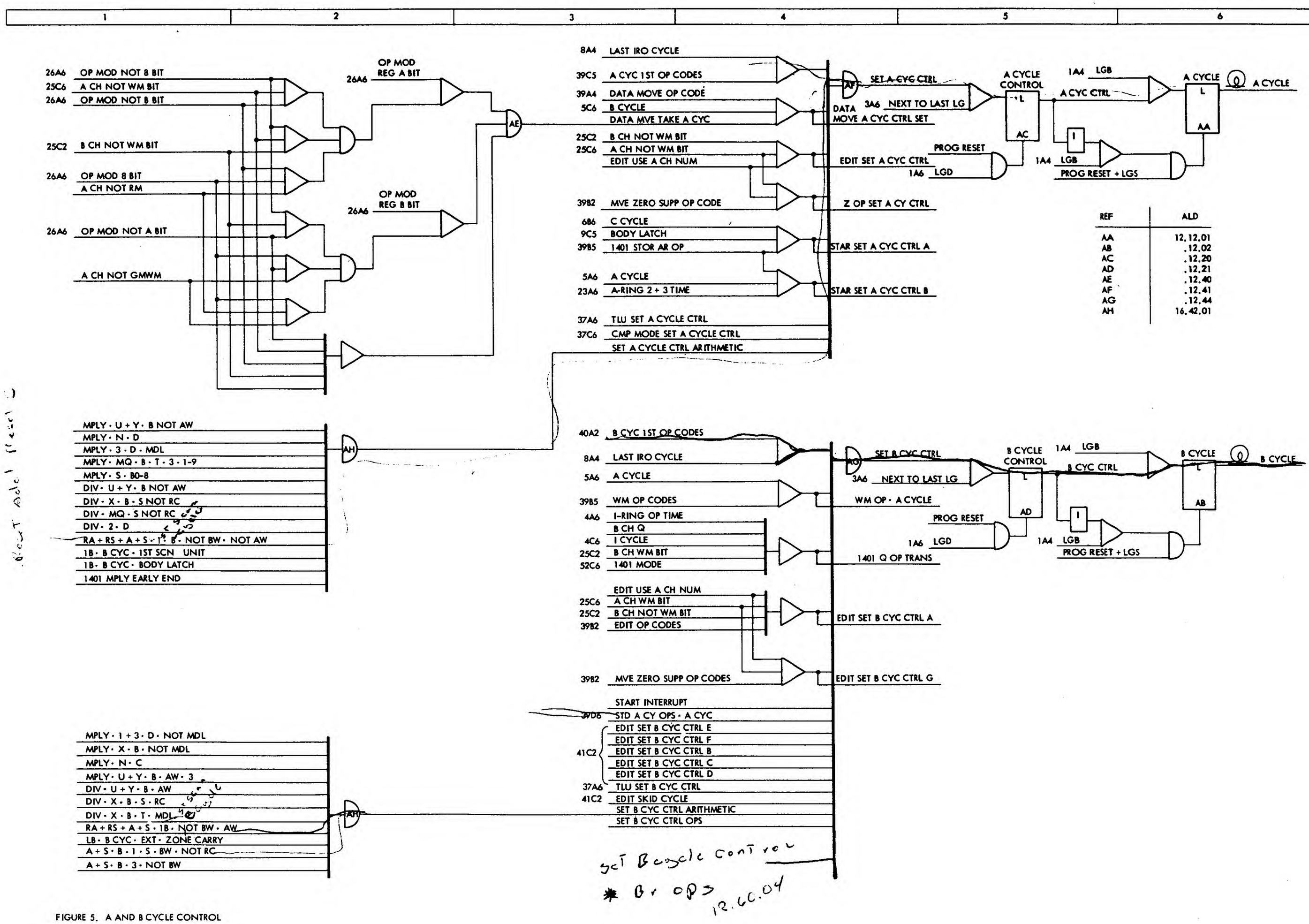
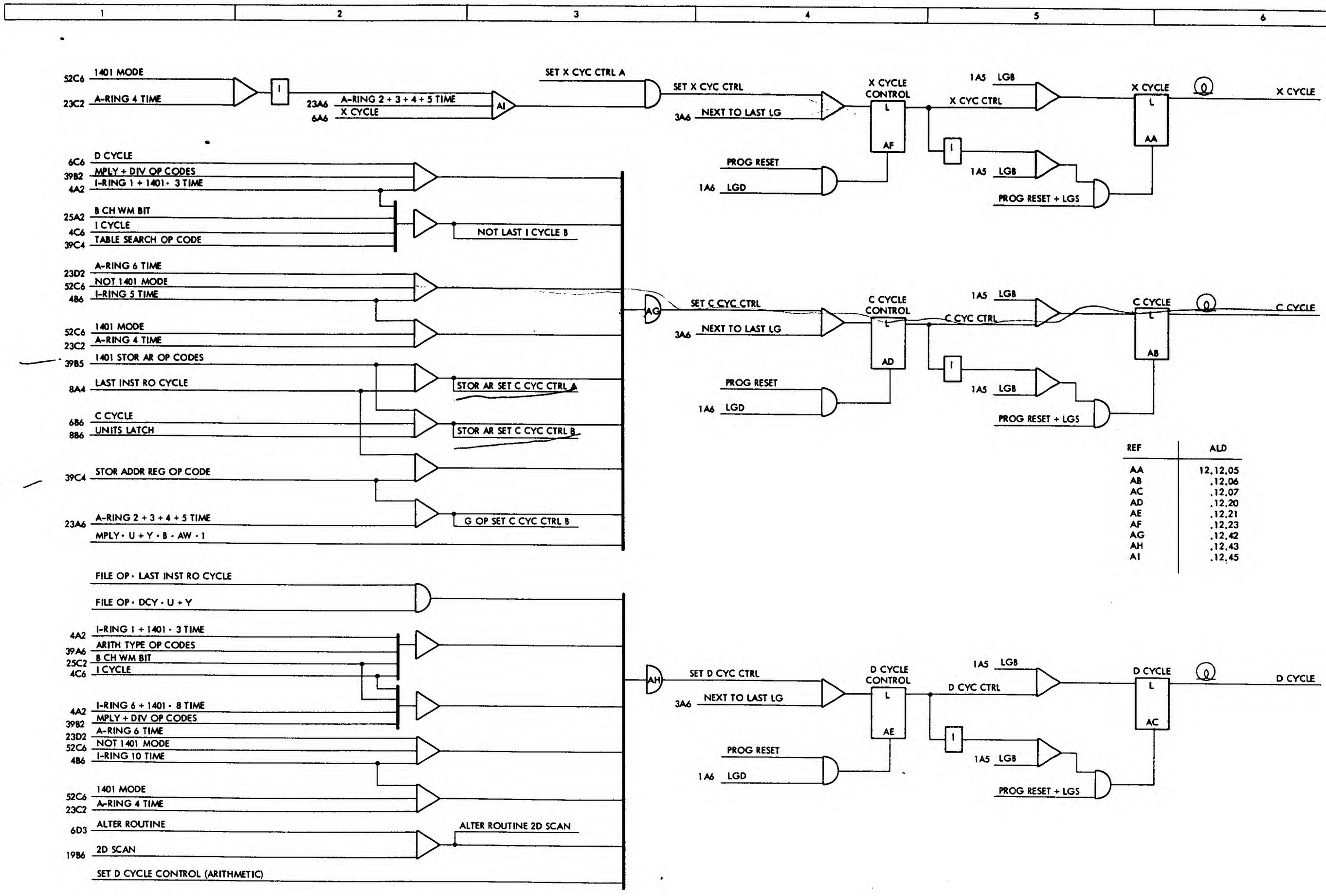


FIGURE 5. A AND B CYCLE CONTROL



REF	ALD
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AB	.12,06
AC	.12,07
AD	.12,20
AE	.12,21
AF	.12,23
AG	.12,42
AH	.12,43
AI	.12,45

FIGURE 6. X, C, AND D CYCLE CONTROL

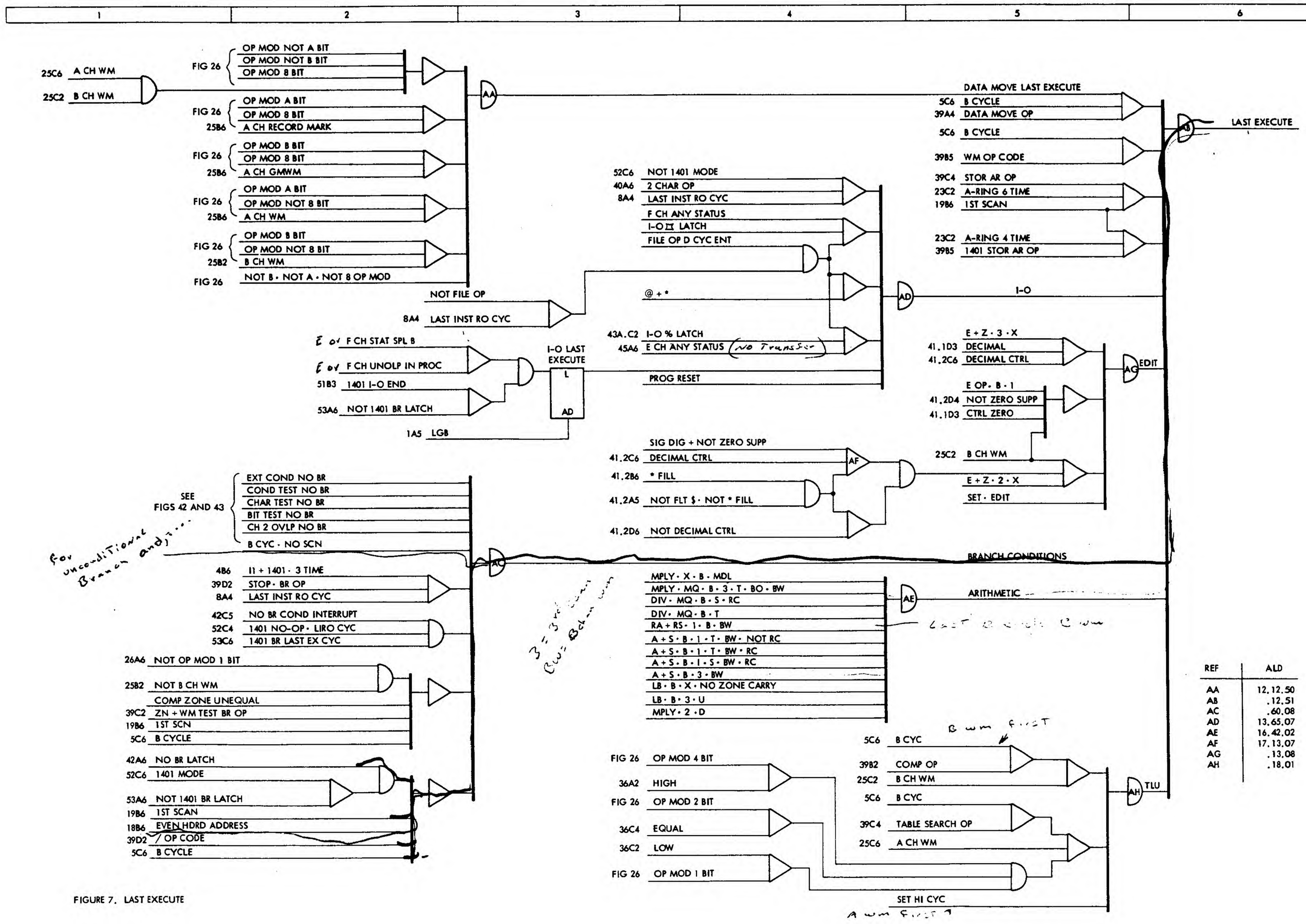
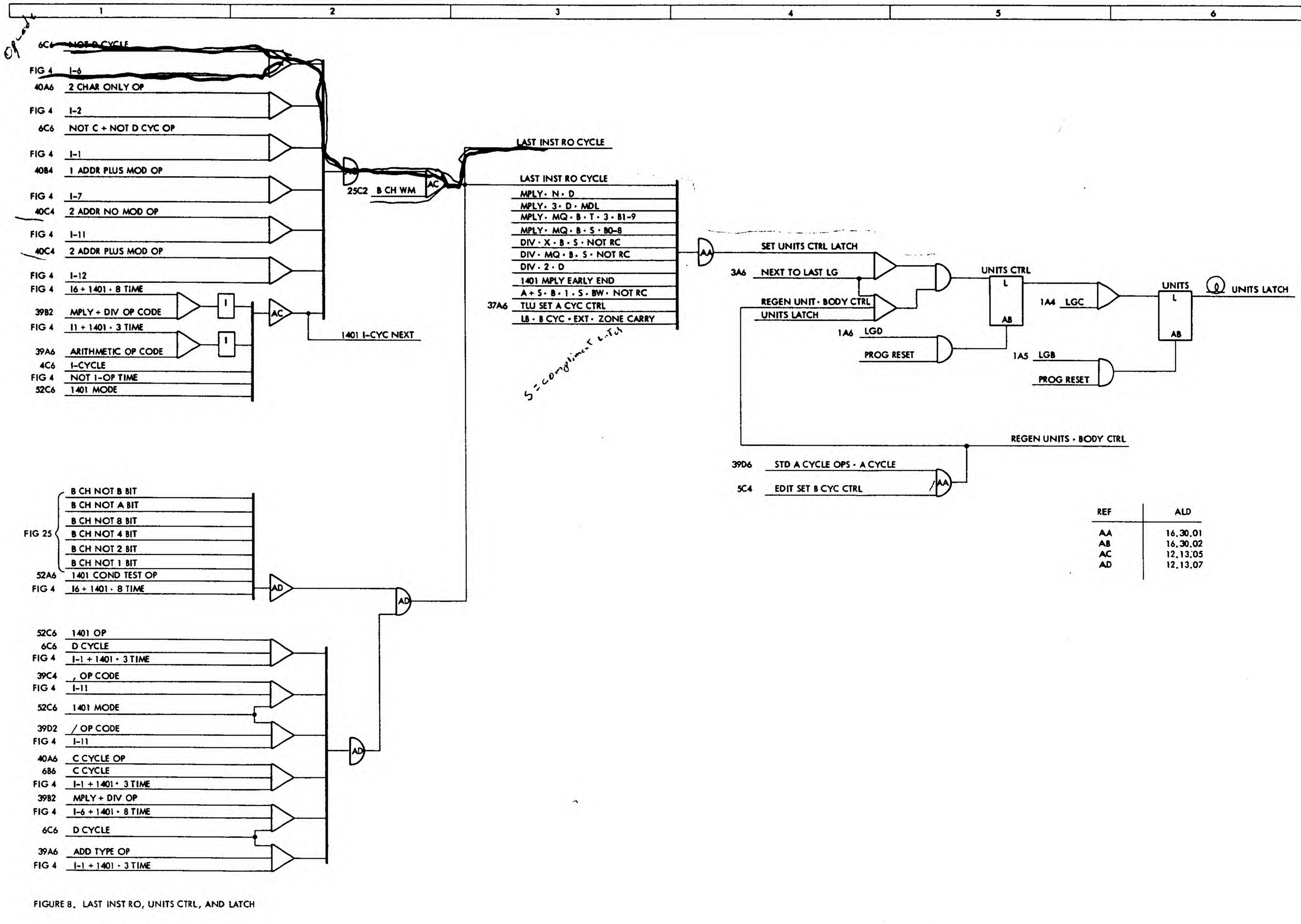


FIGURE 7. LAST EXECUTE



REF	ALD
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AB	16.30.02
AC	12.13.05
AD	12.13.07

FIGURE 8. LAST INST RO, UNITS CTRL, AND LATCH

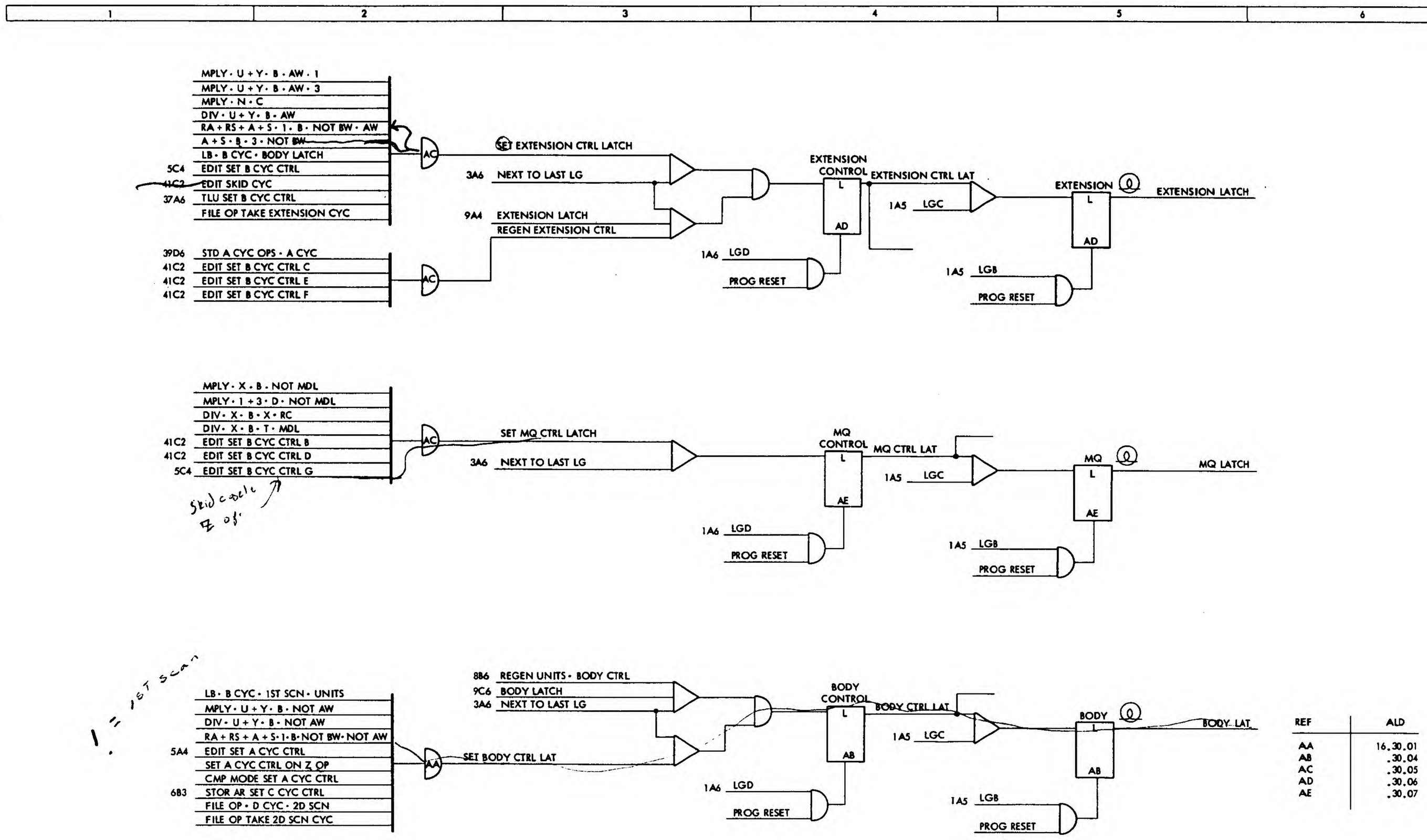


FIGURE 9. BODY, EXTENSION, MQ LATCH

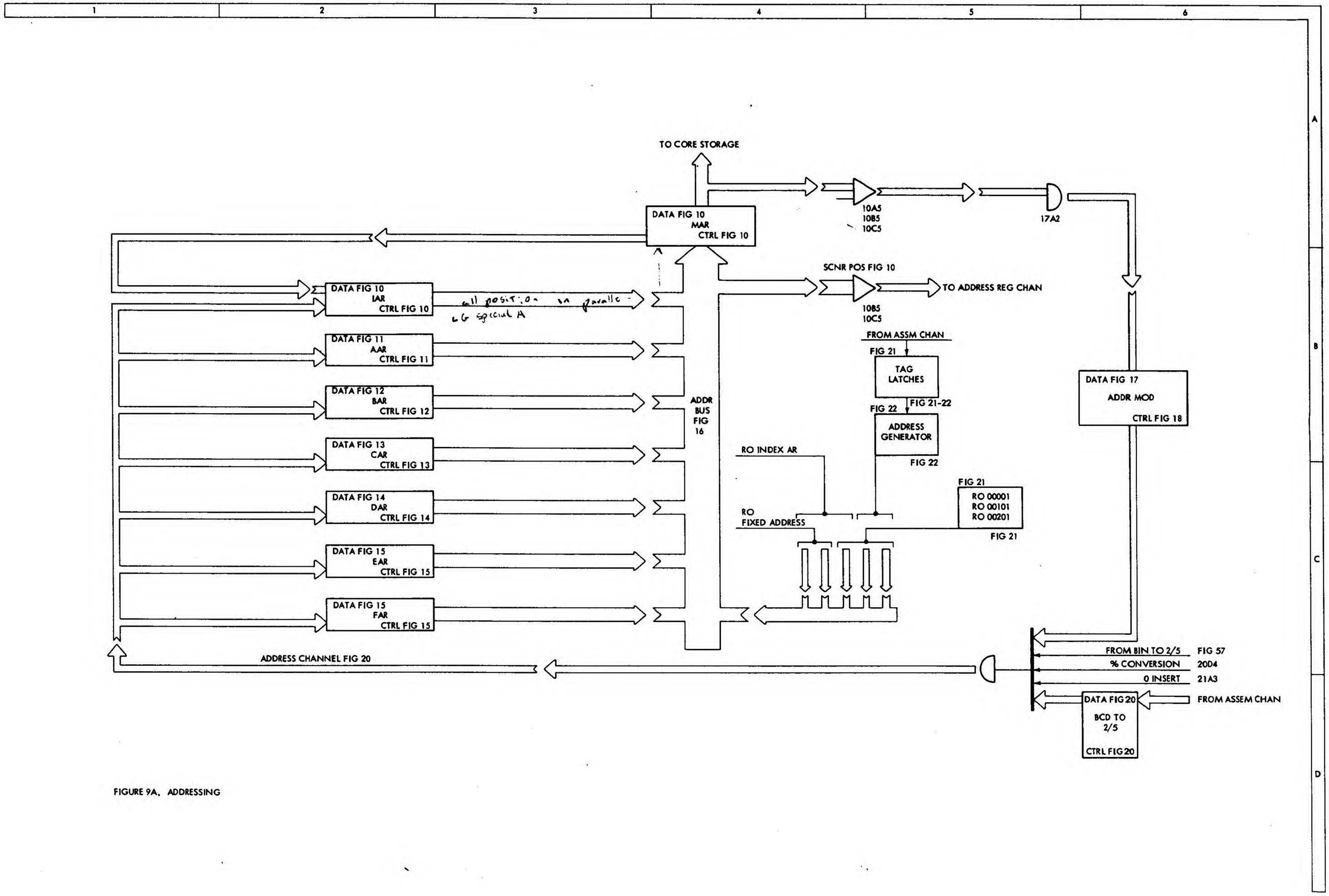


FIGURE 9A. ADDRESSING

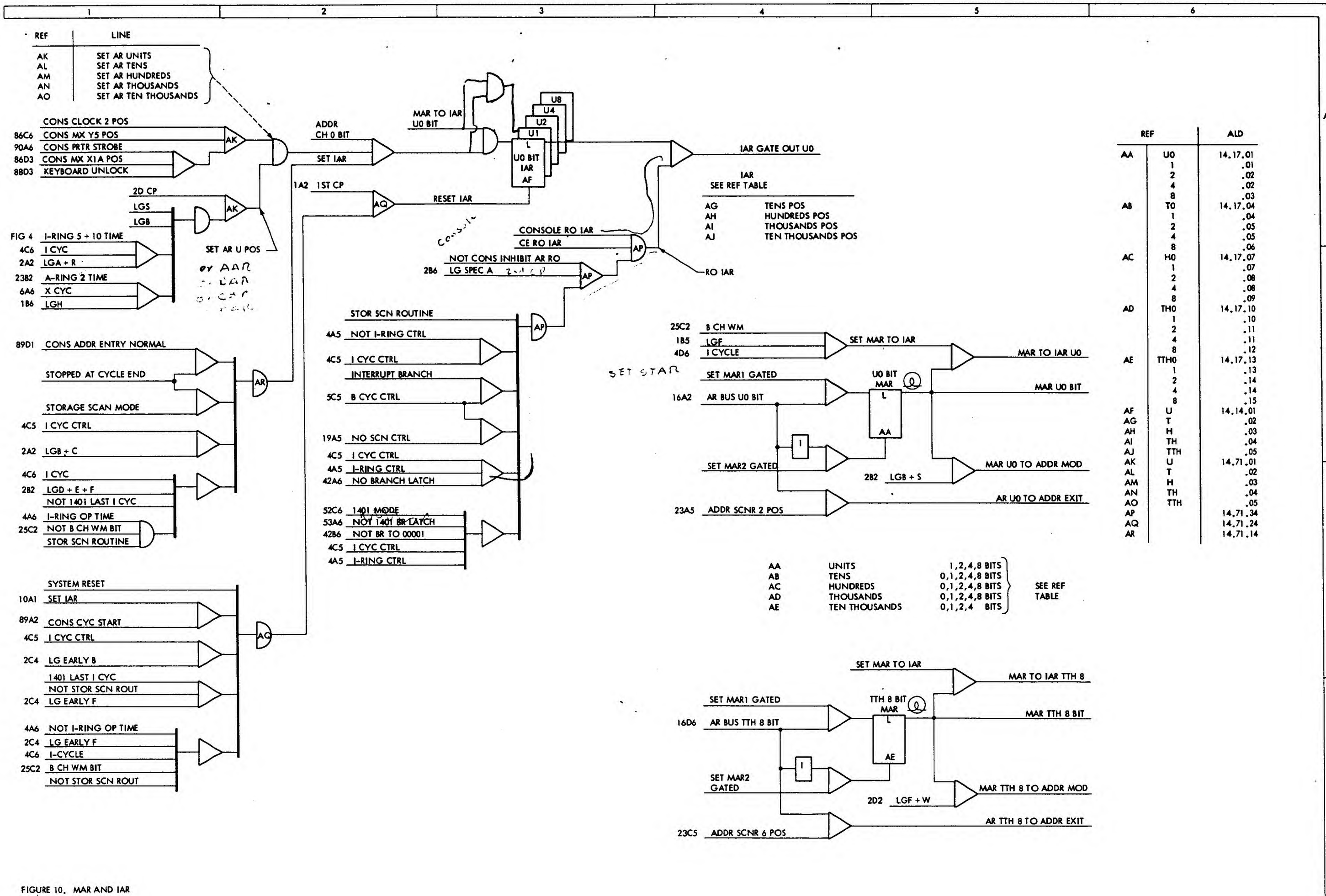
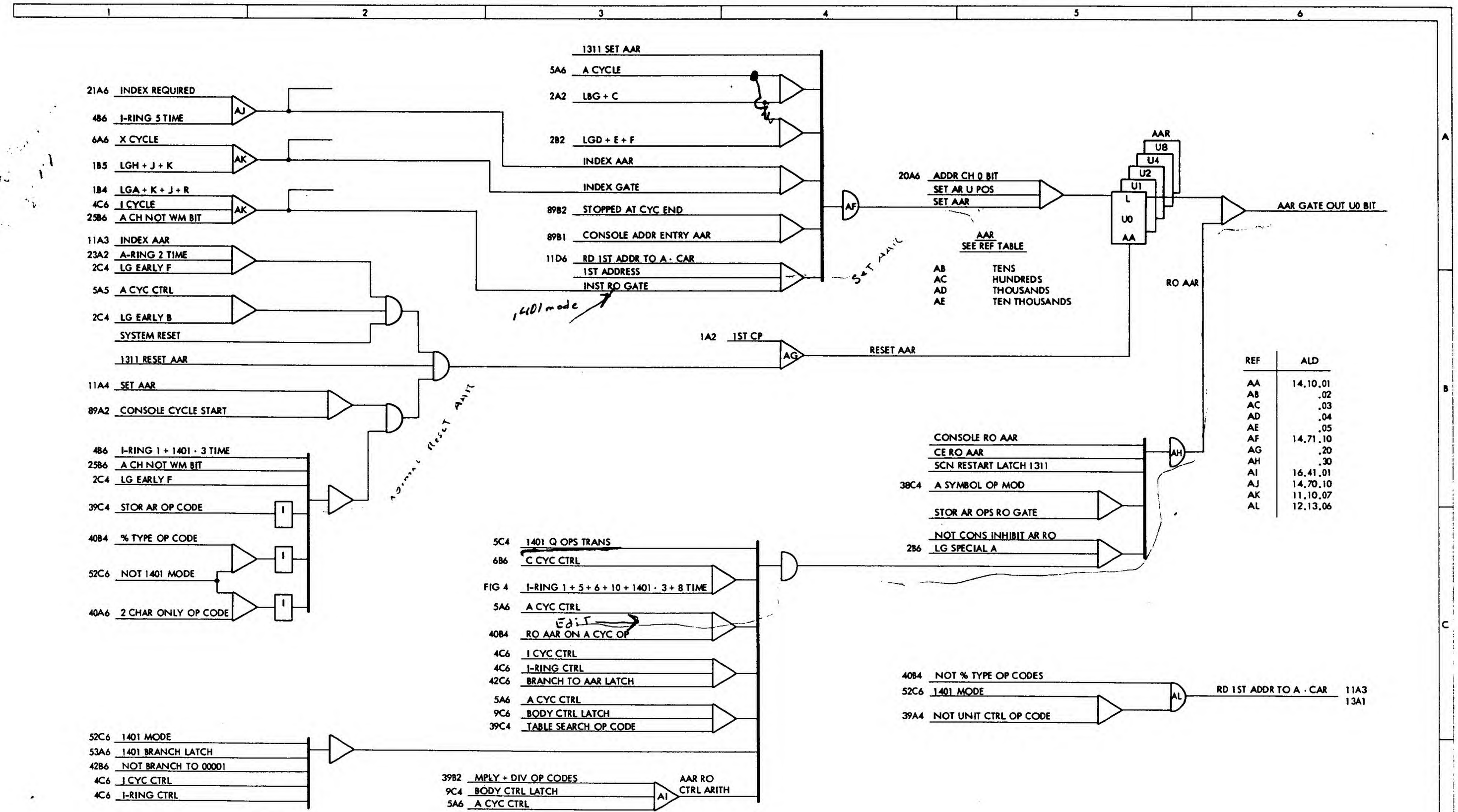


FIGURE 10. MAR AND IAR



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AB	.02
AC	.03
AD	.04
AE	.05
AF	14.71.10
AG	.20
AH	.30
AI	16.41.01
AJ	14.70.10
AK	11.10.07
AL	12.13.06

FIGURE 11. AAR

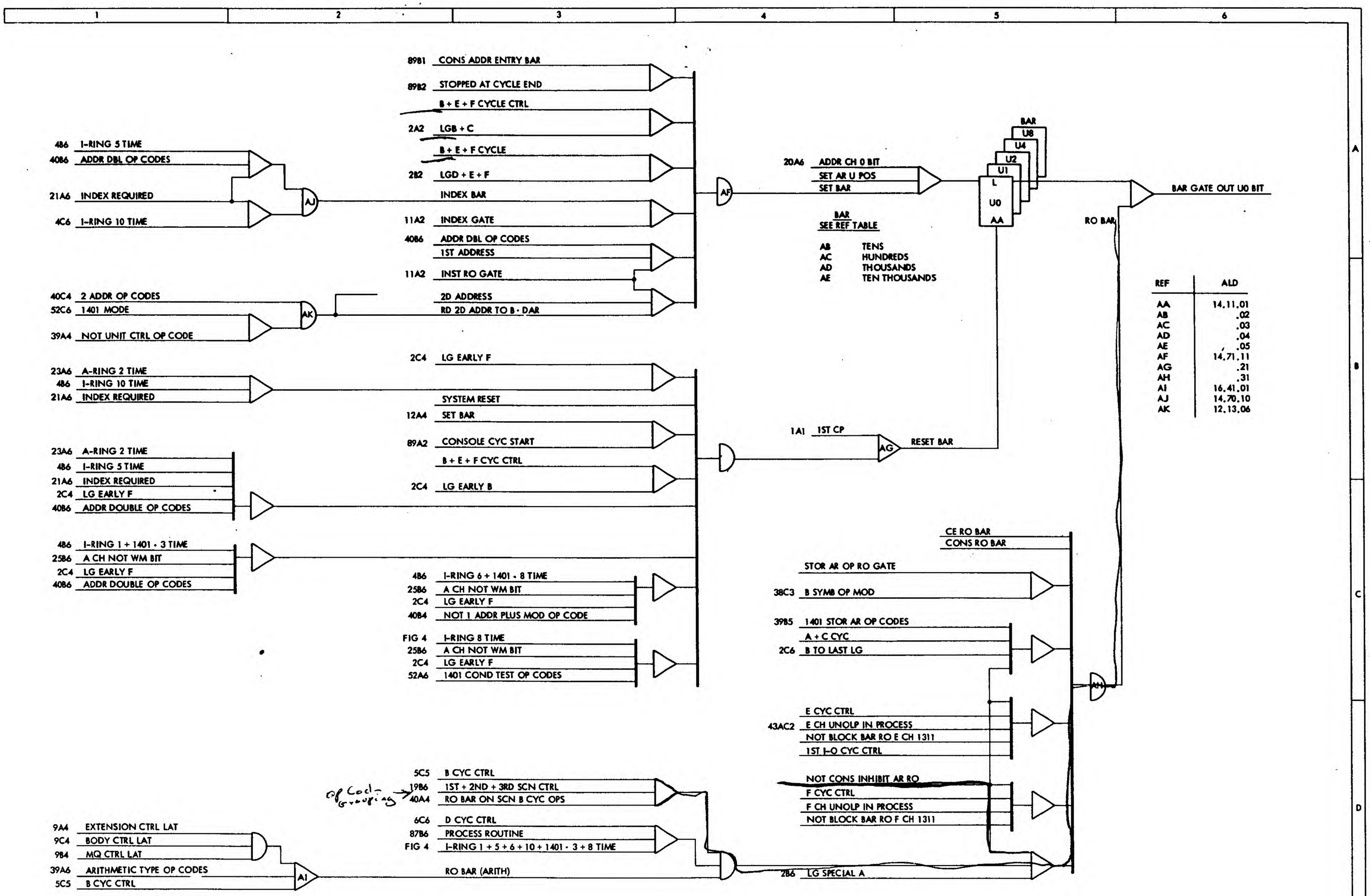


FIGURE 12. BAR

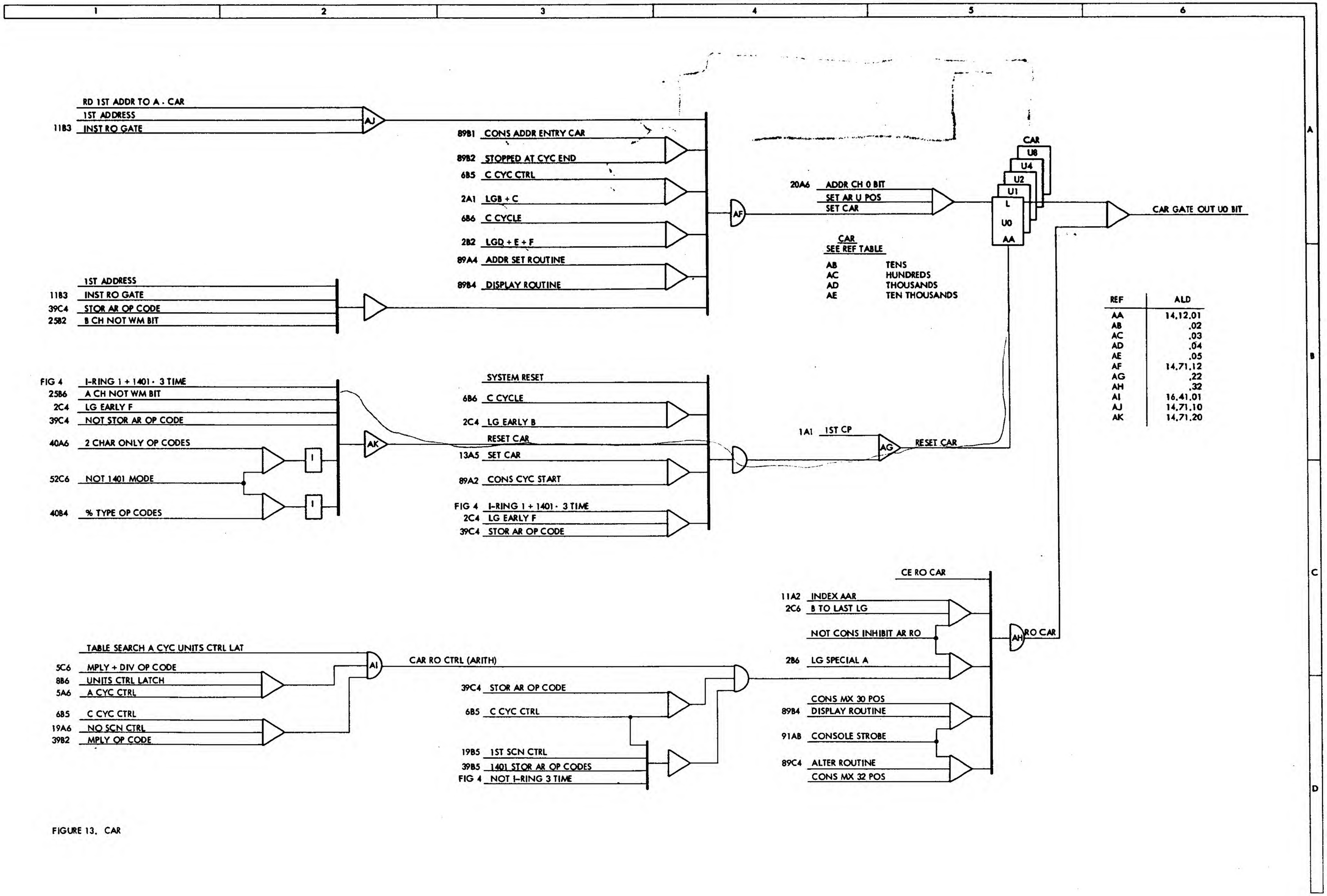


FIGURE 13. CAR

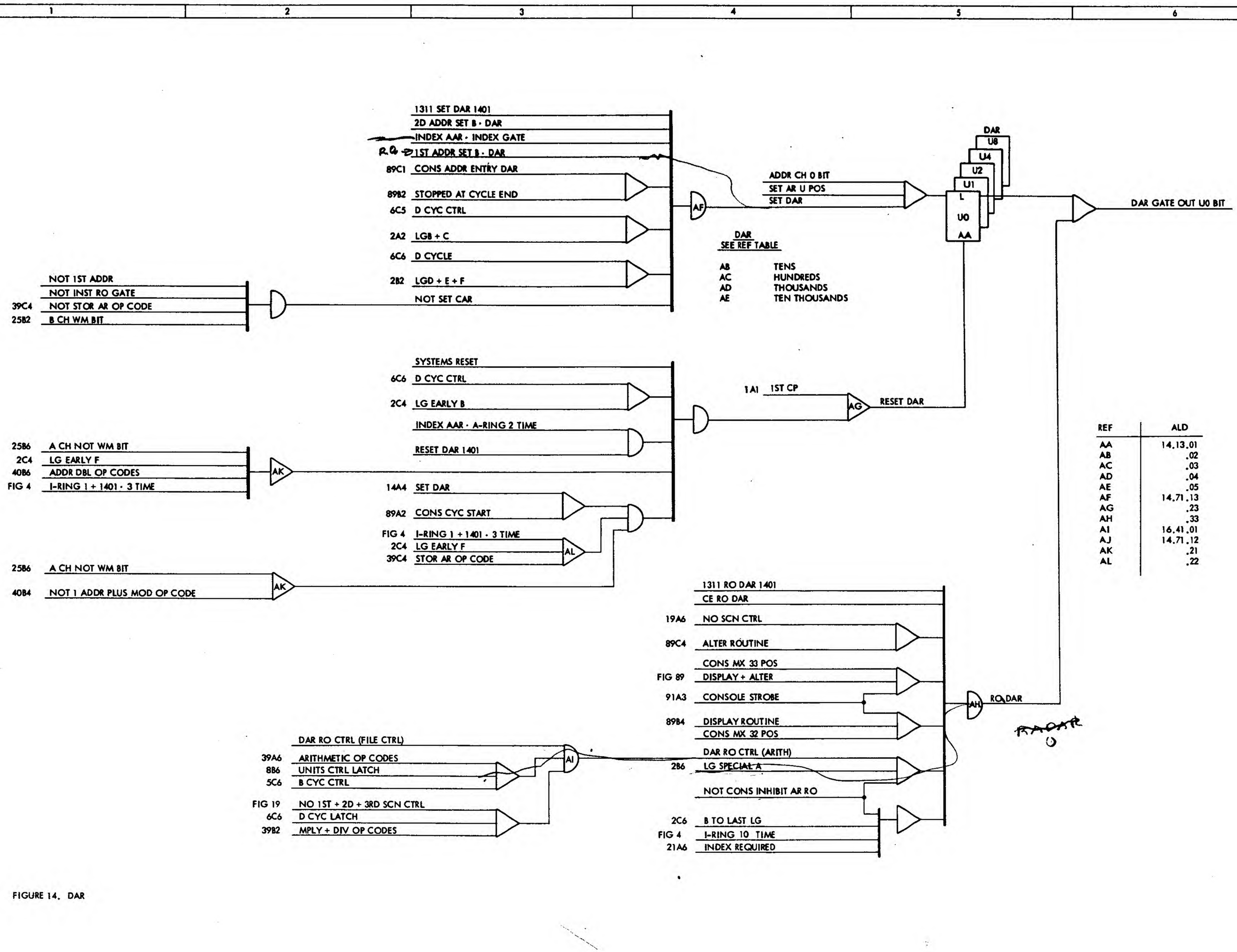


FIGURE 14. DAR

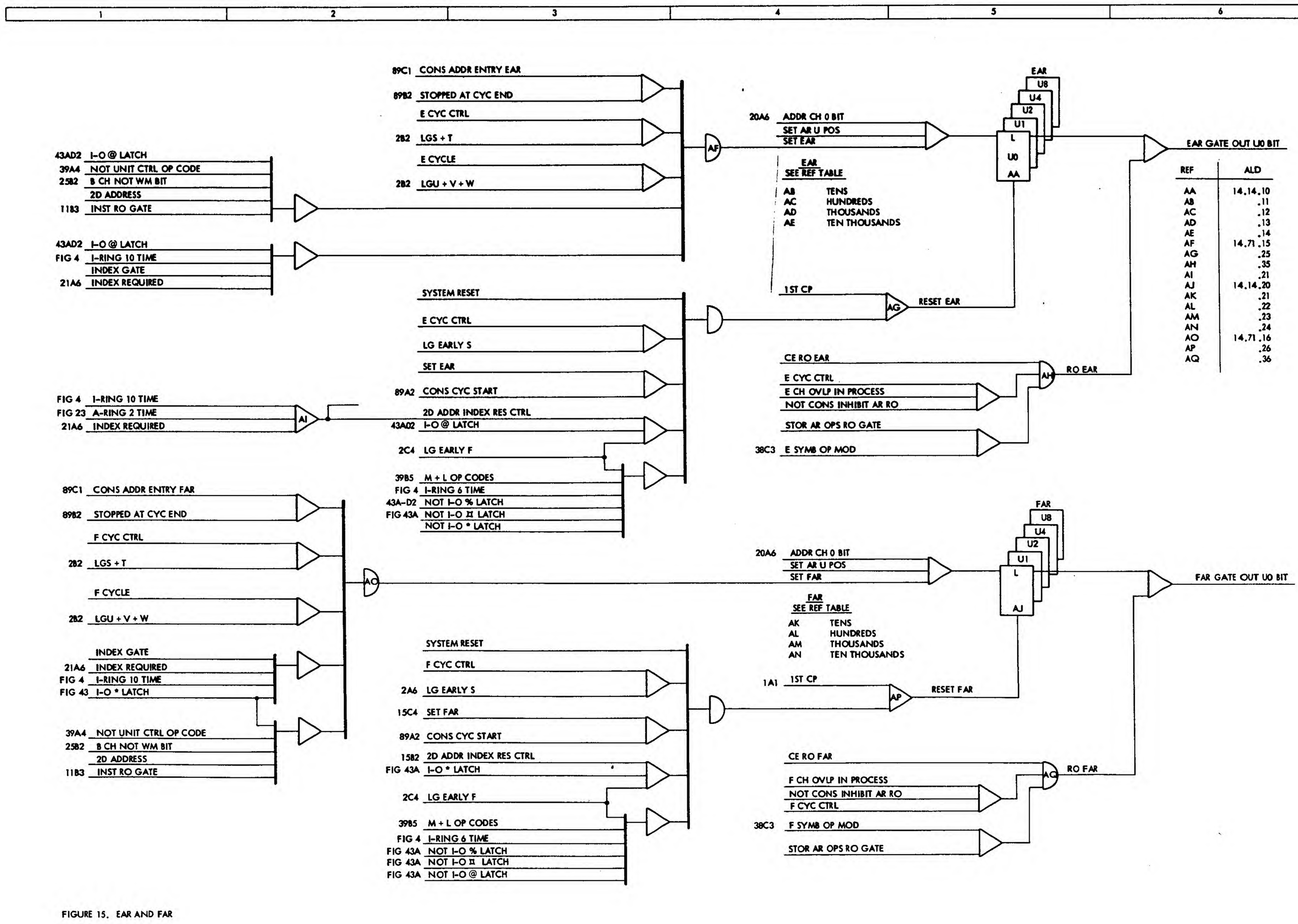


FIGURE 15. EAR AND FAR

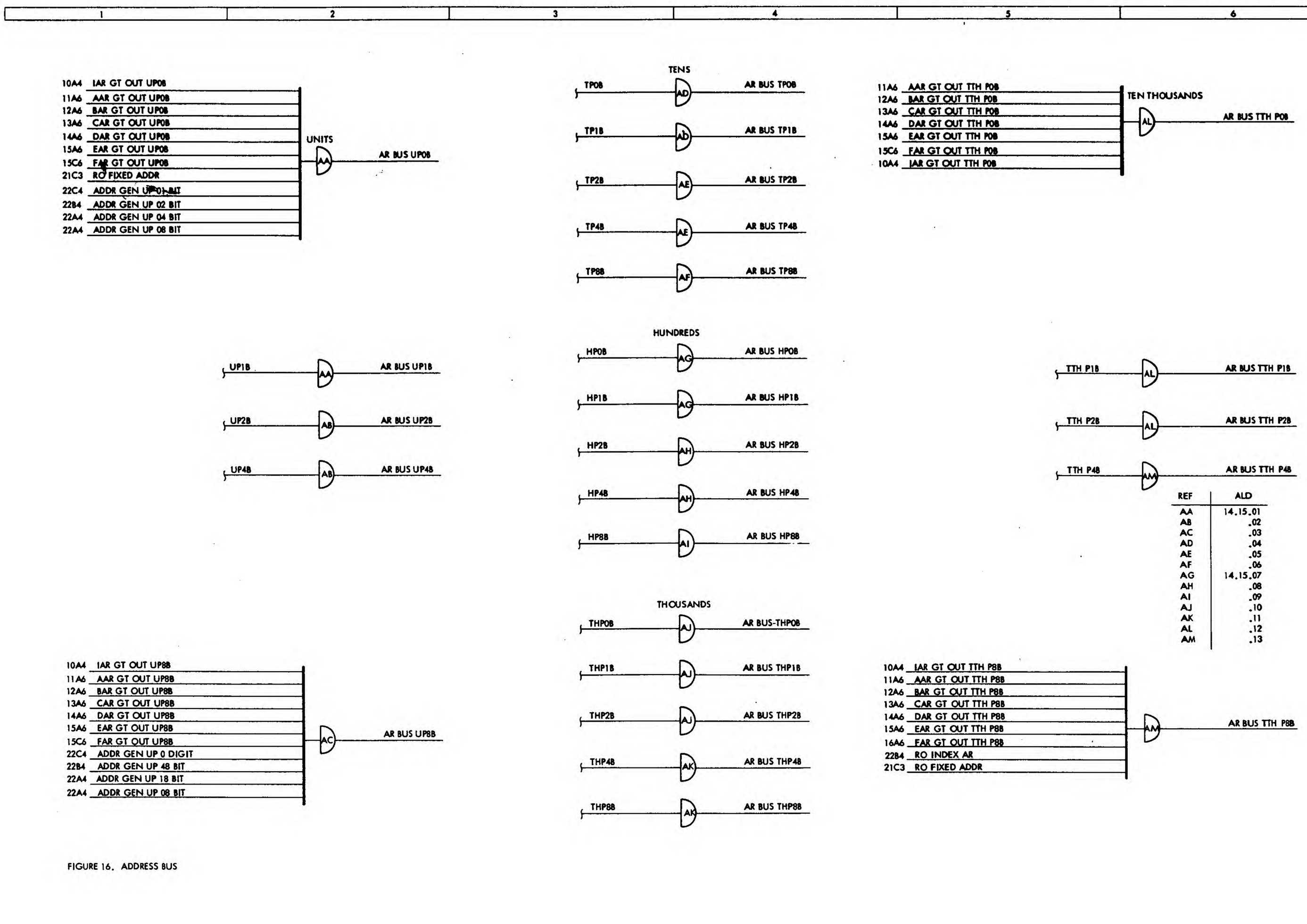


FIGURE 16. ADDRESS BUS

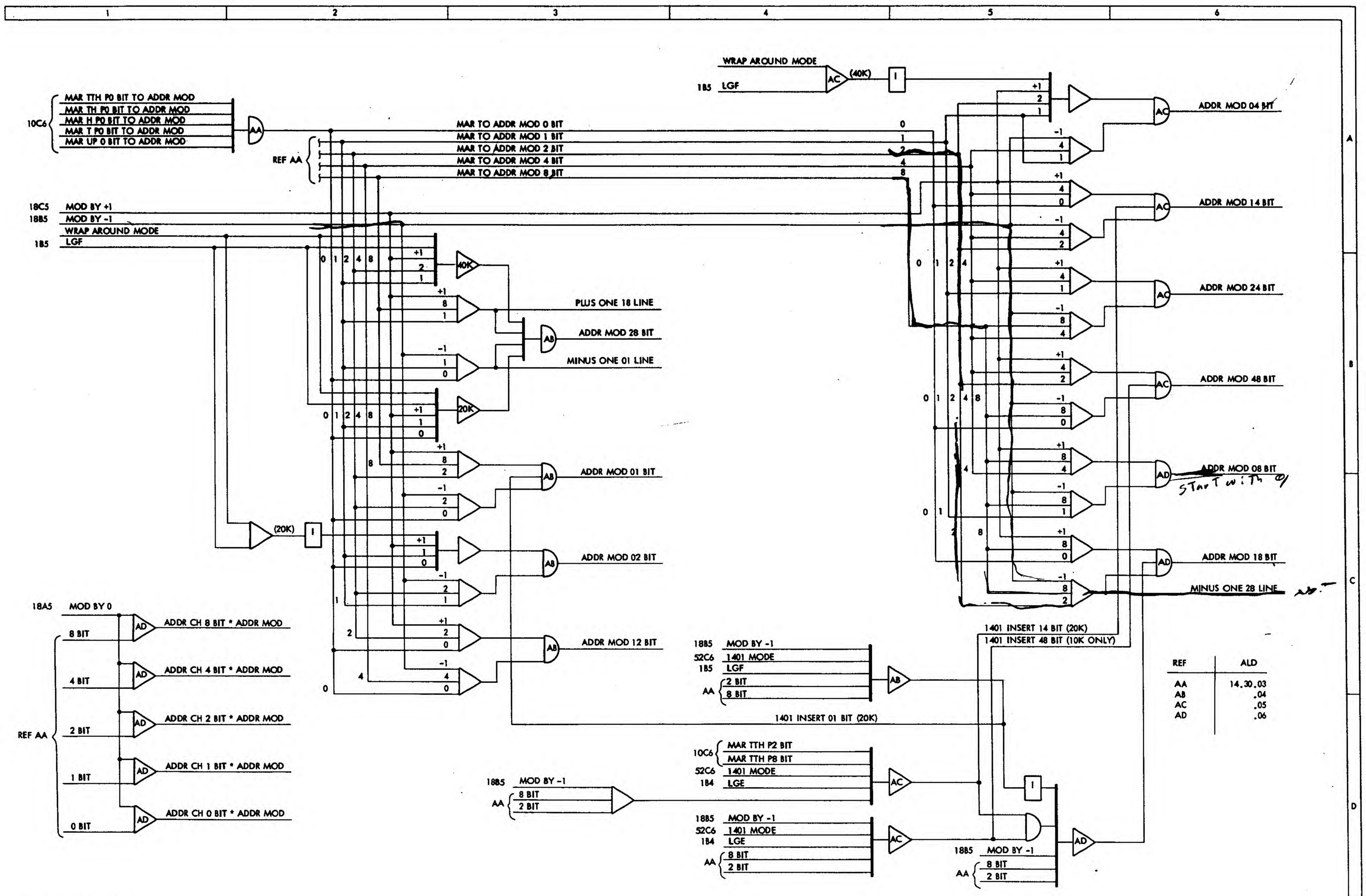


FIGURE 17. ADDR MOD

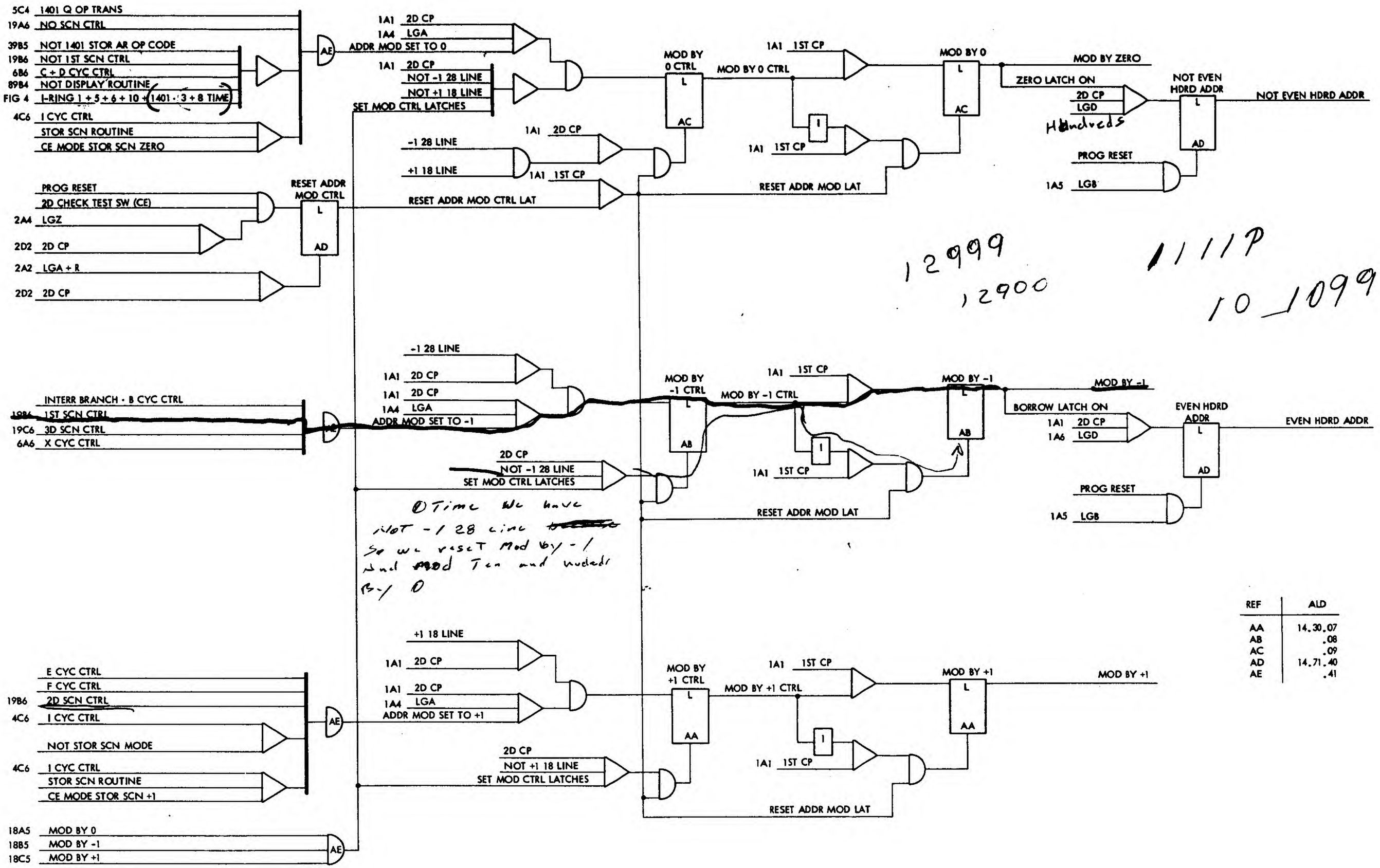


FIGURE 18. ADDRESS MOD CONTROL

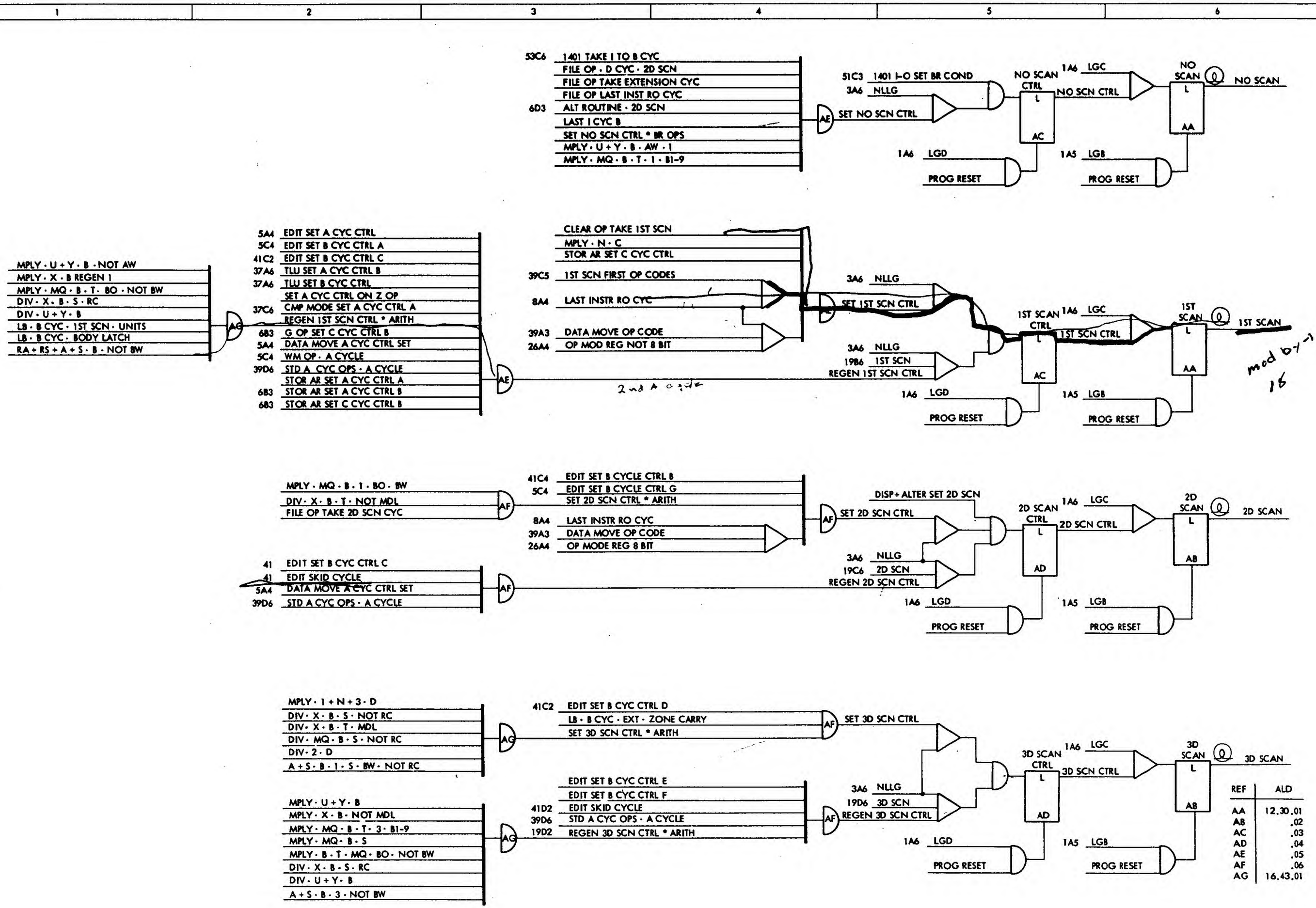


FIGURE 19. SCAN LATCHES AND CTRLS

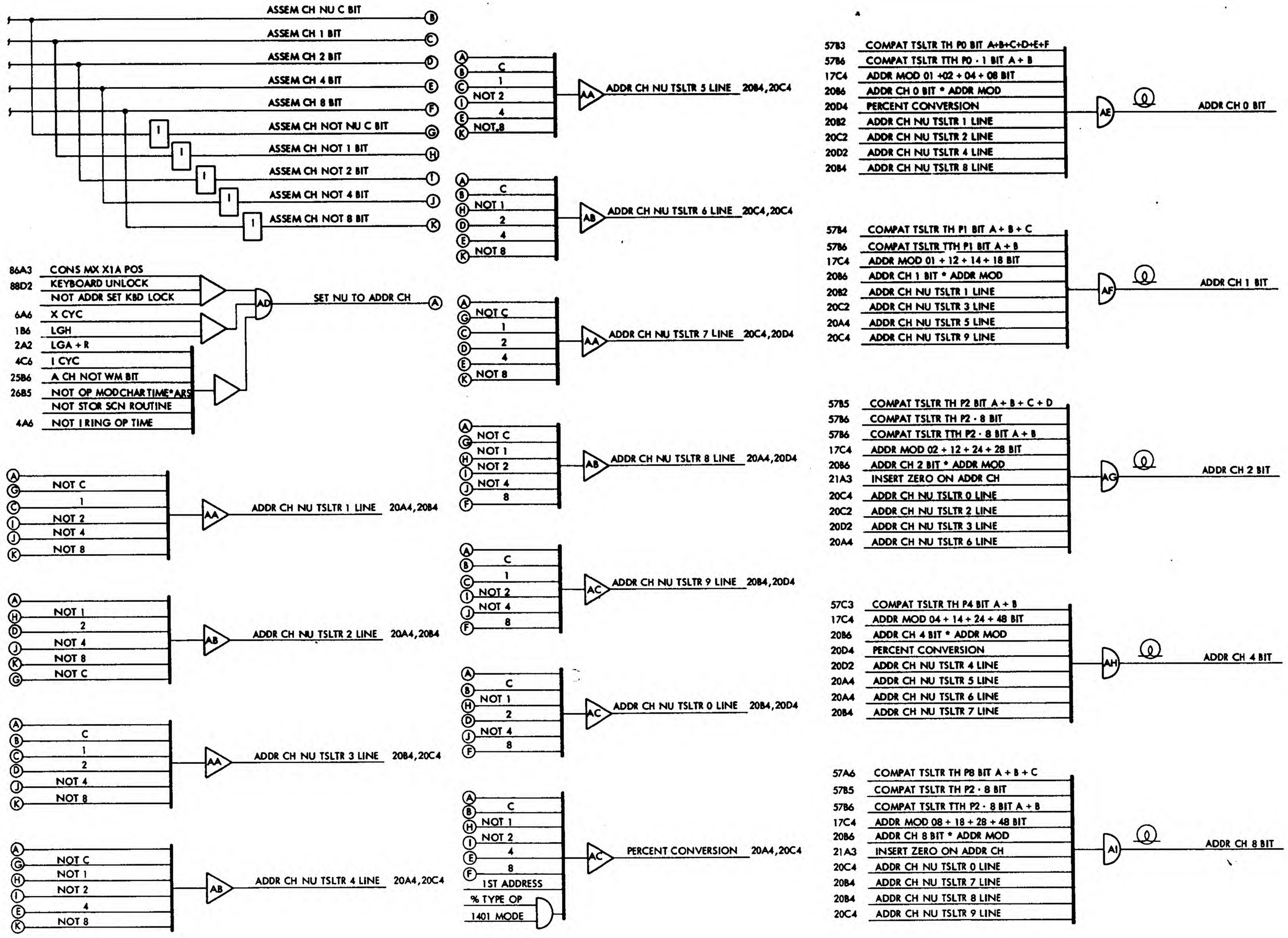


FIGURE 20. BCD TO 2/5 AND ADDR CH

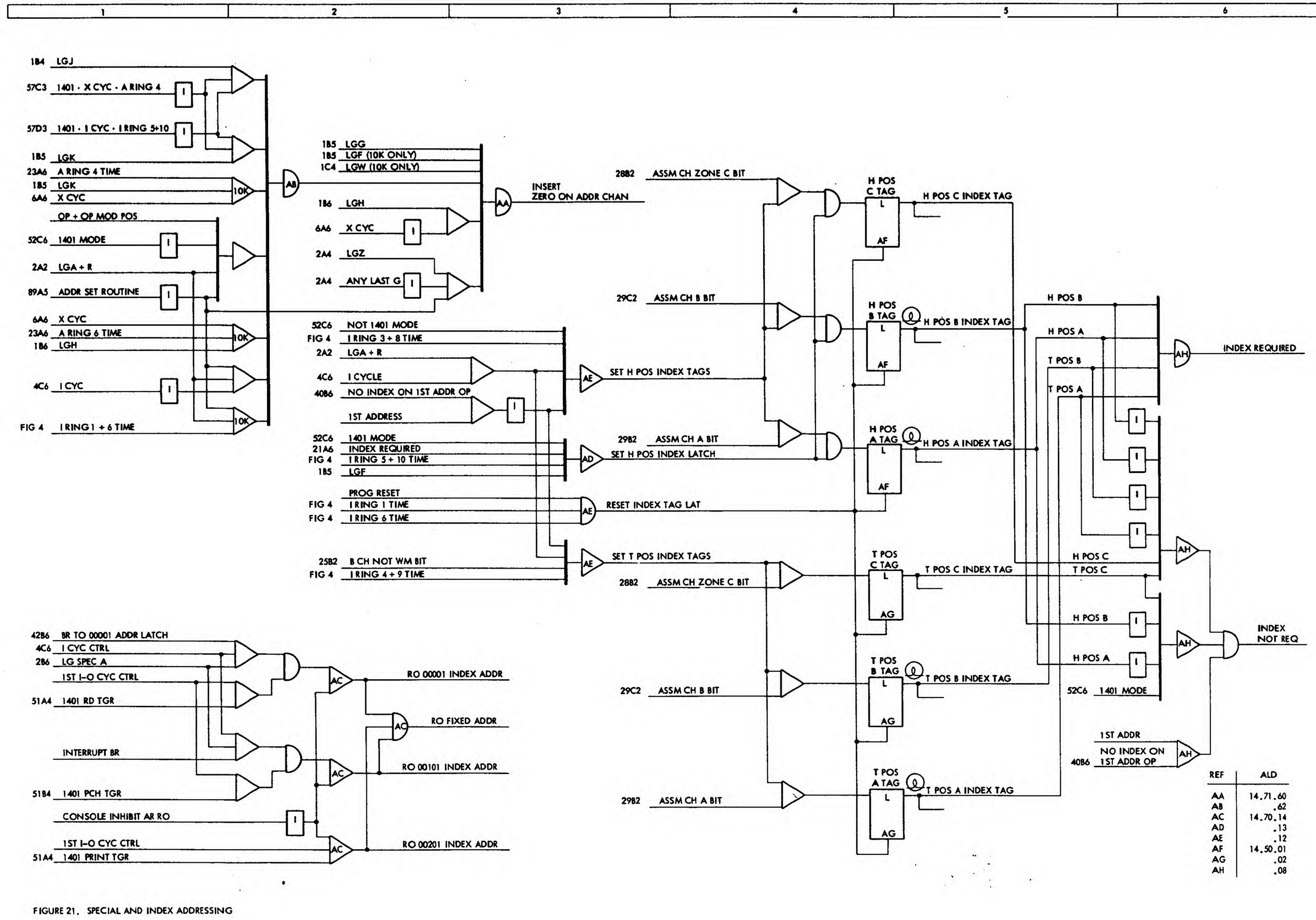
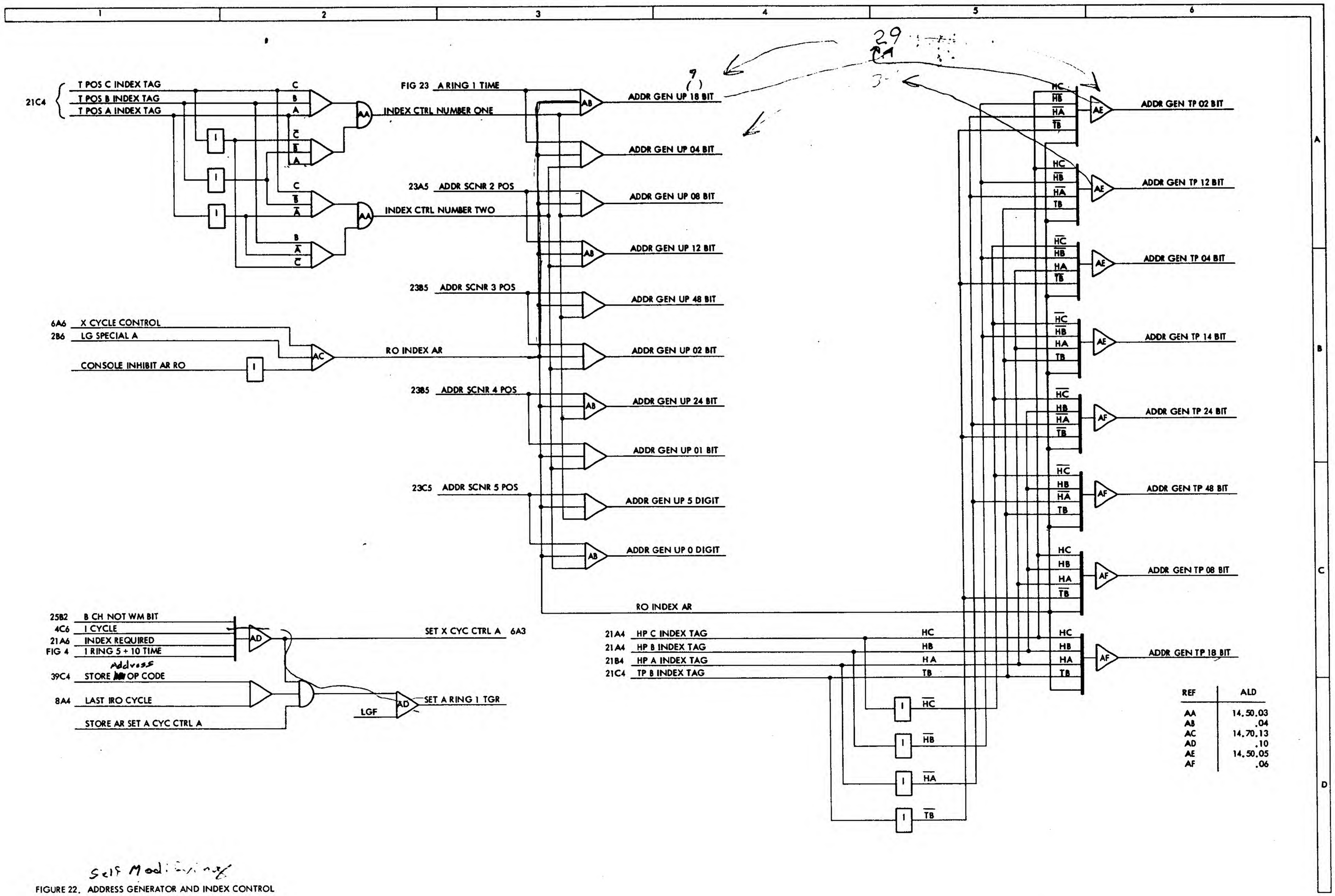
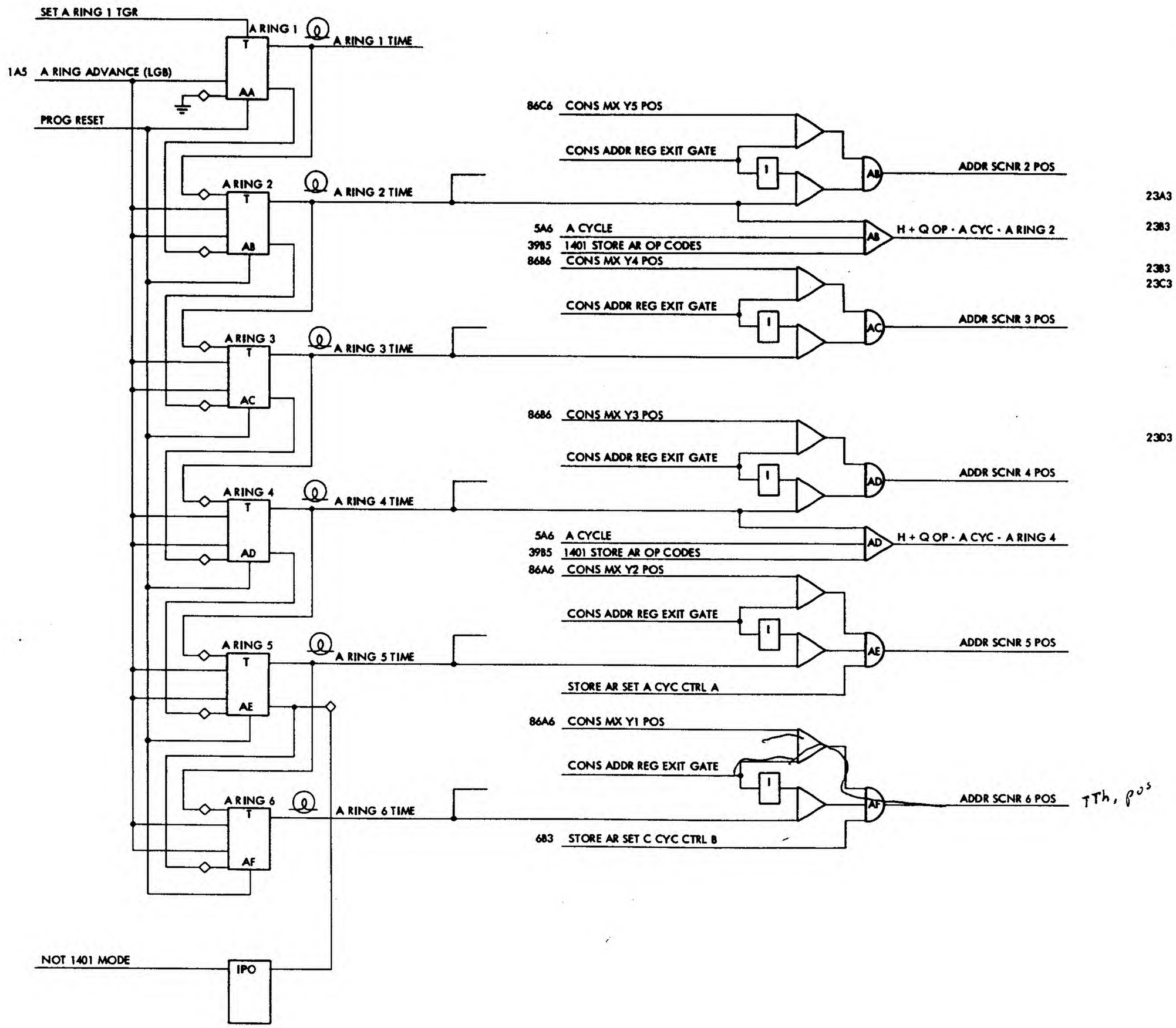


FIGURE 21. SPECIAL AND INDEX ADDRESSING



Self Modifying

FIGURE 22. ADDRESS GENERATOR AND INDEX CONTROL



REF	ALD
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AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	.07

FIGURE 23. A RING AND ADDRESS SCNR

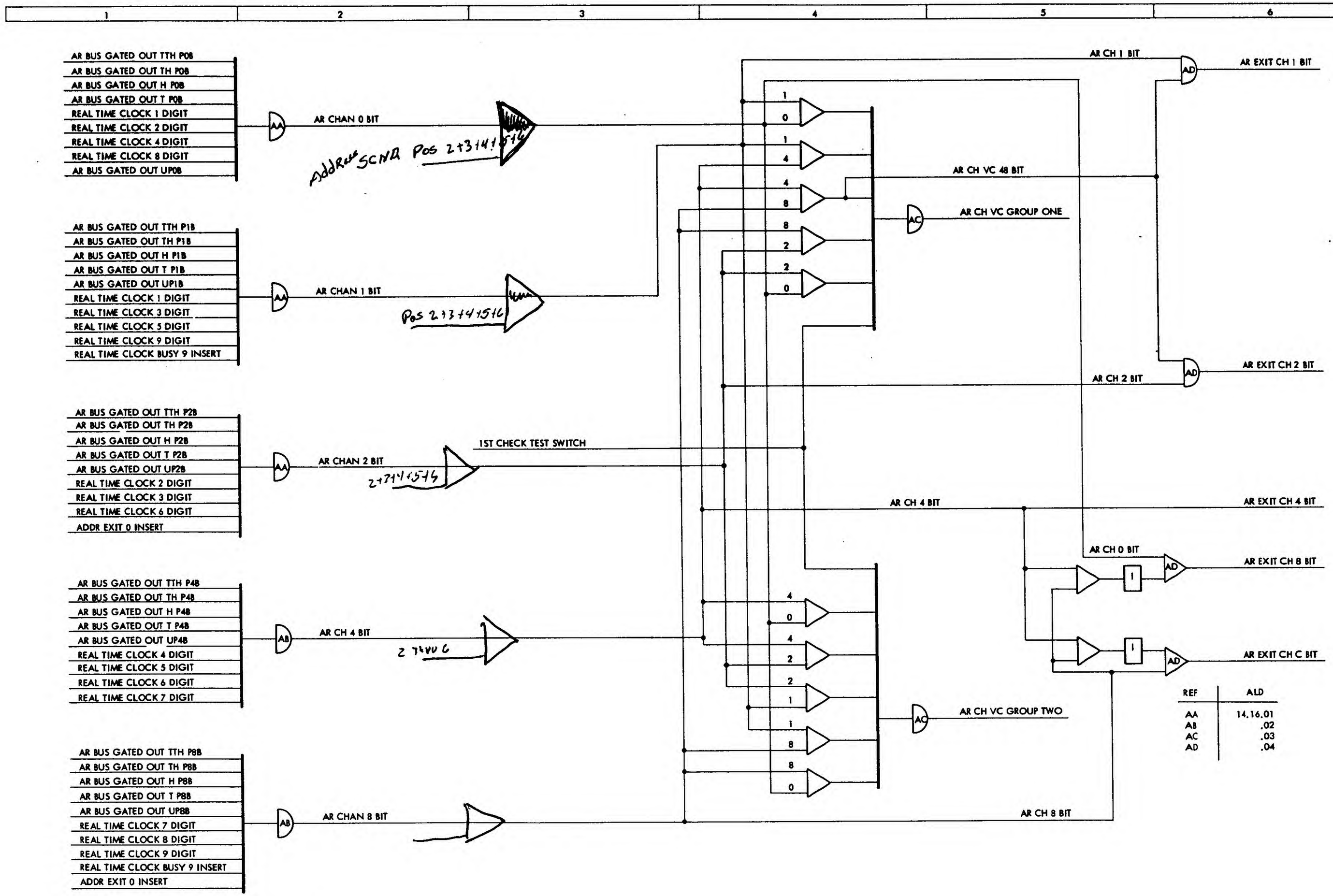


FIGURE 24. ADDR REG AND ADDR EXIT CHAN, 2/5 - BCD

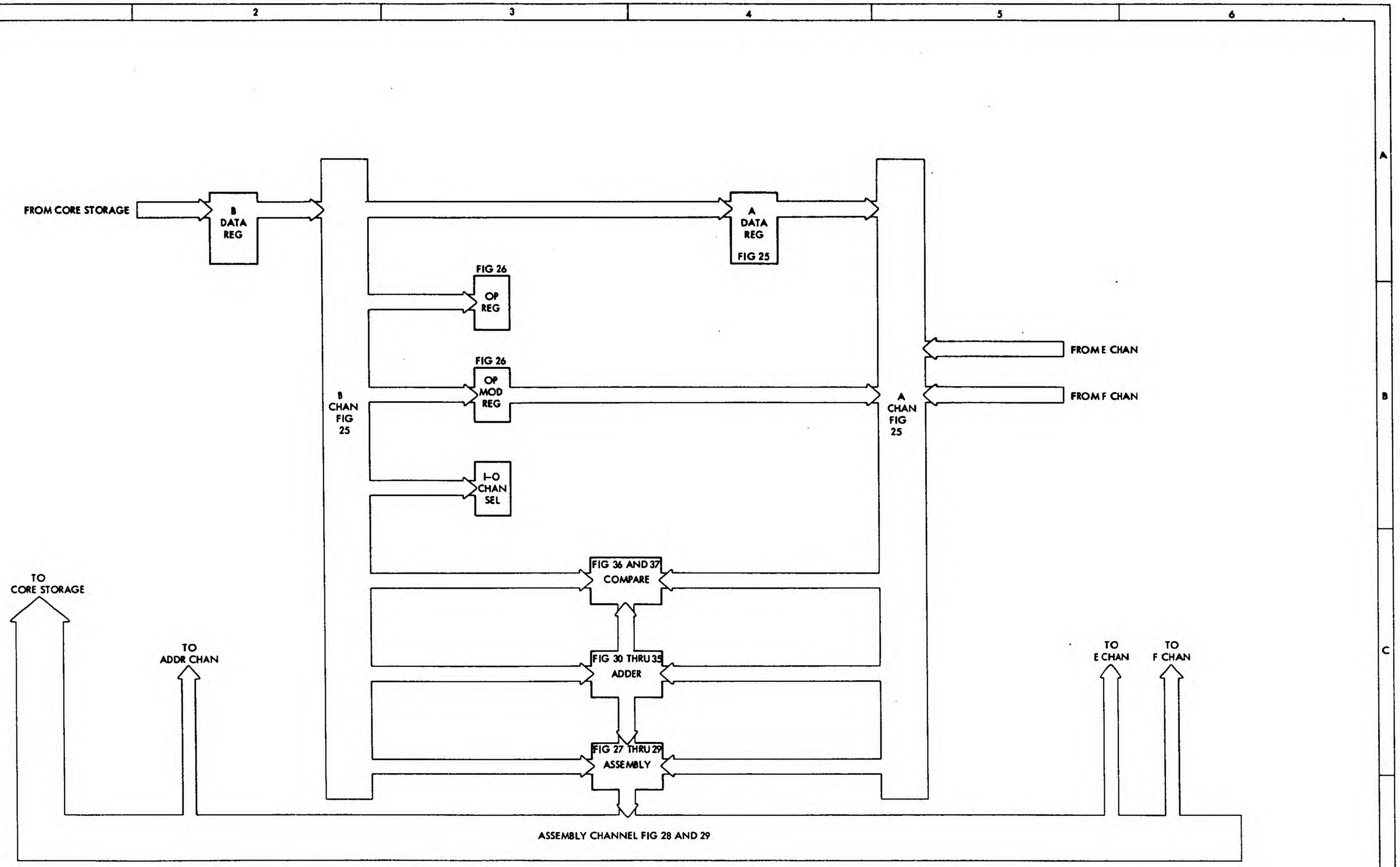


FIGURE 24A. A AND B CHANNEL

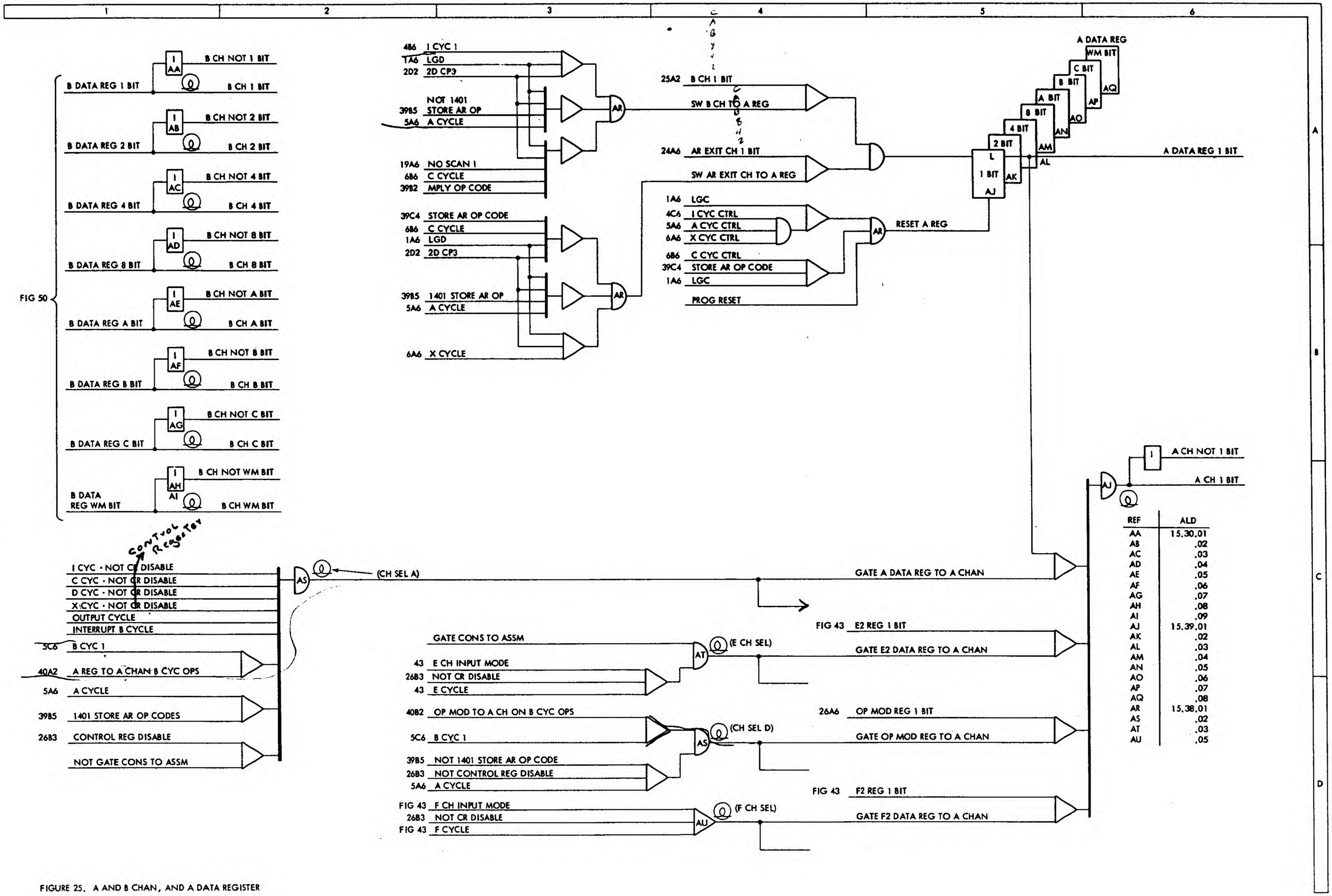


FIGURE 25. A AND B CHAN, AND A DATA REGISTER

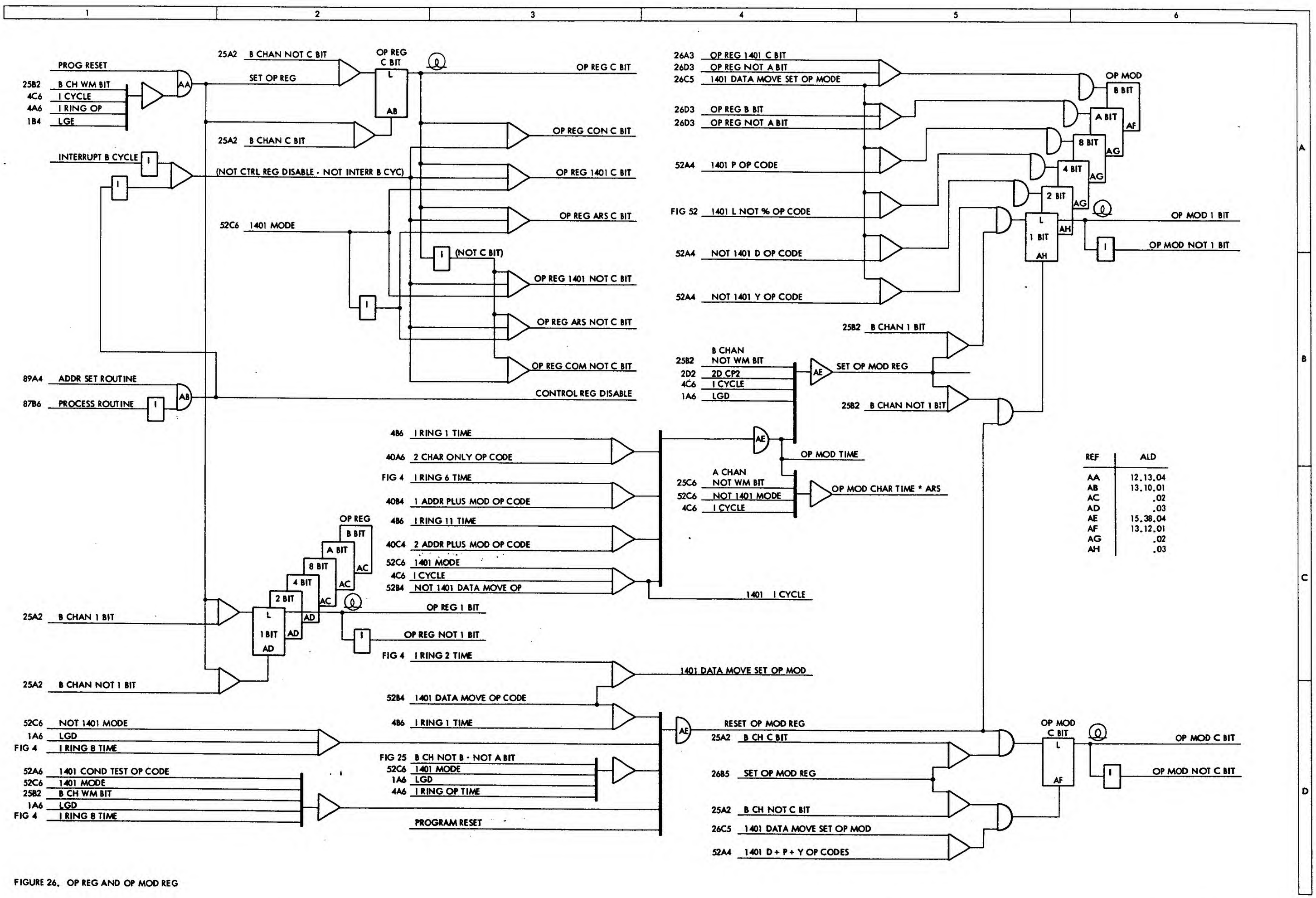


FIGURE 26. OP REG AND OP MOD REG

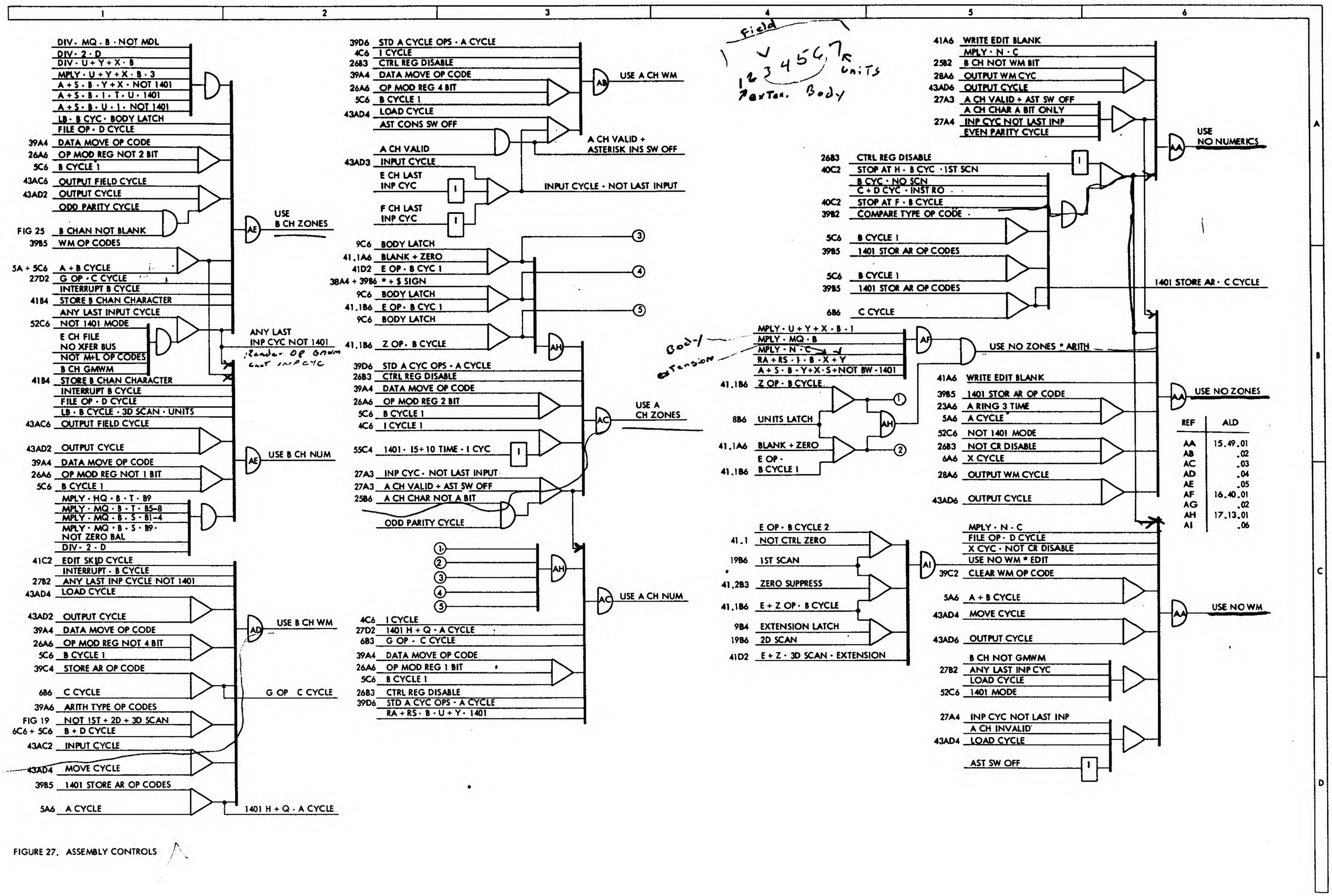
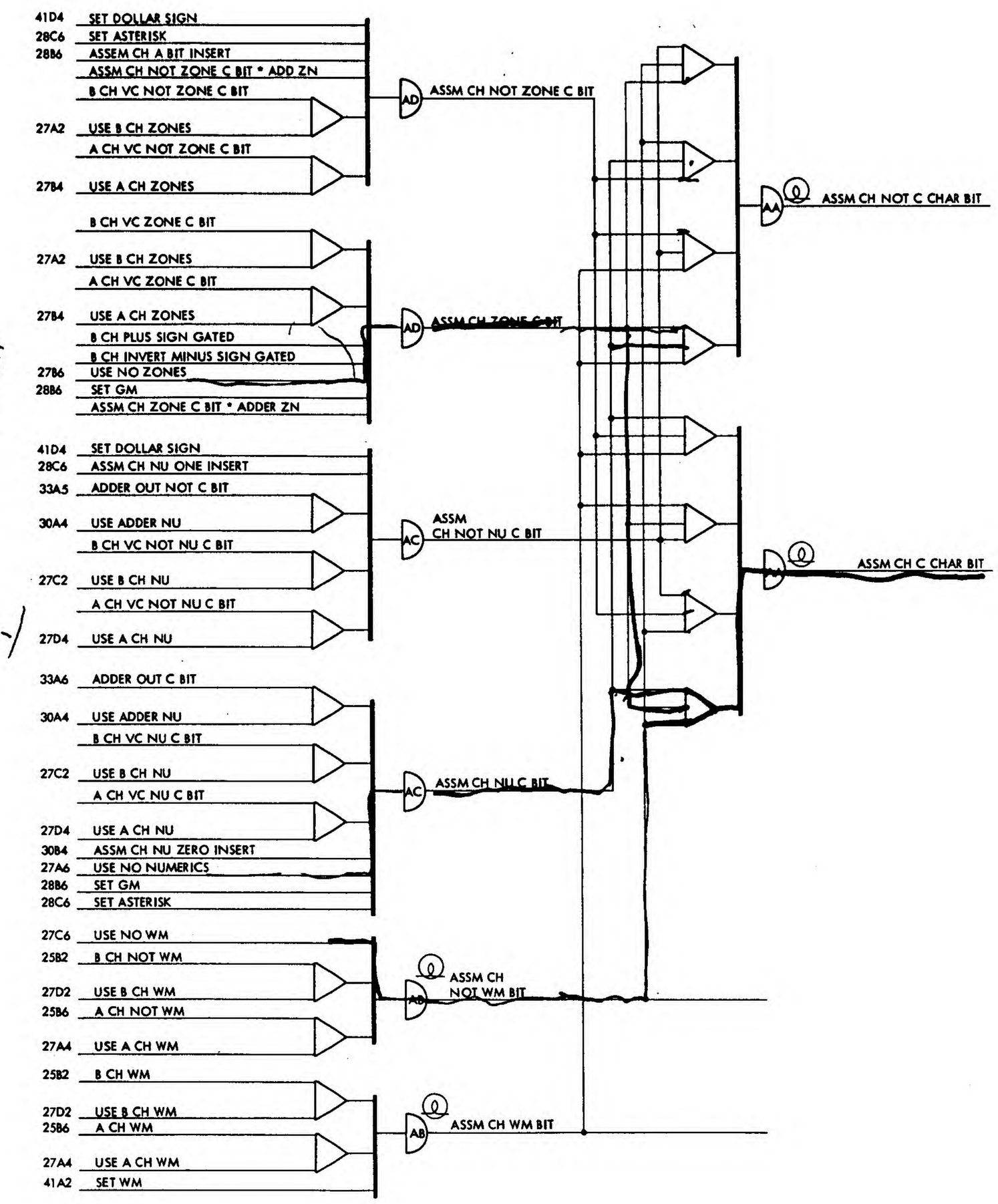
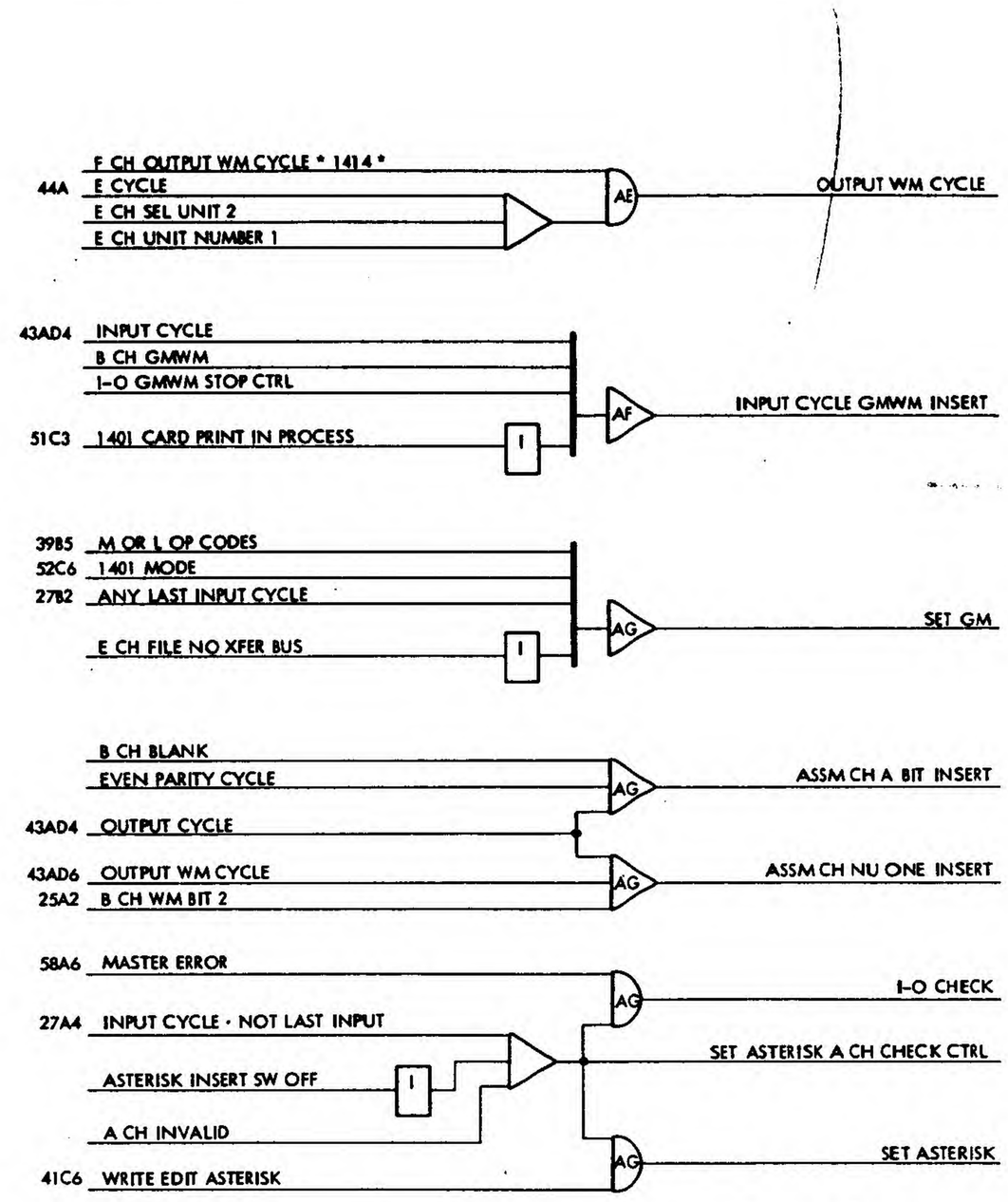


FIGURE 27. ASSEMBLY CONTROLS





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AA	15.50.07
AB	.08
AC	.09
AD	.10
AE	15.49.02
AF	.05
AG	.06

FIGURE 28. ASSEMBLY CHAN C AND WM BIT

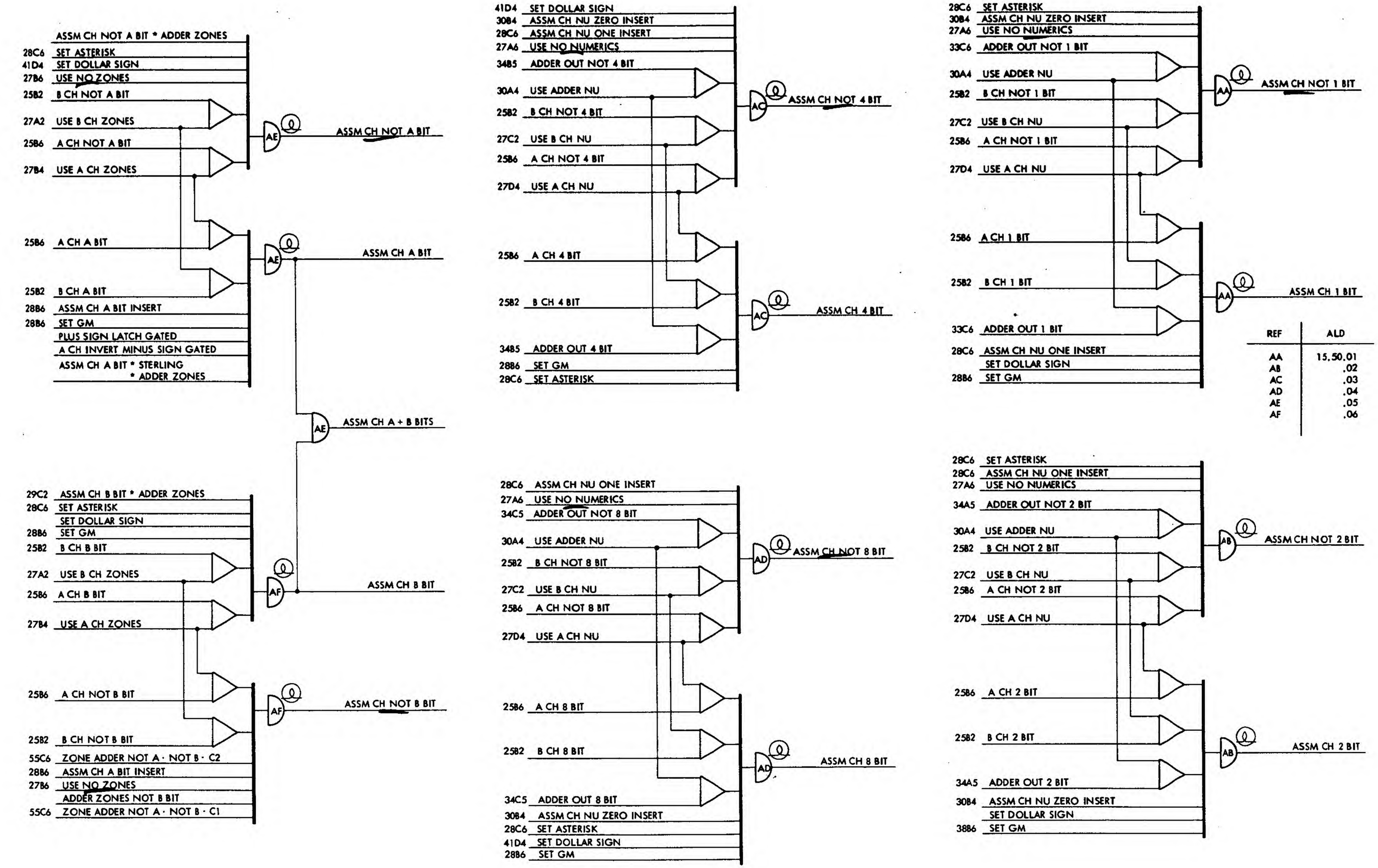
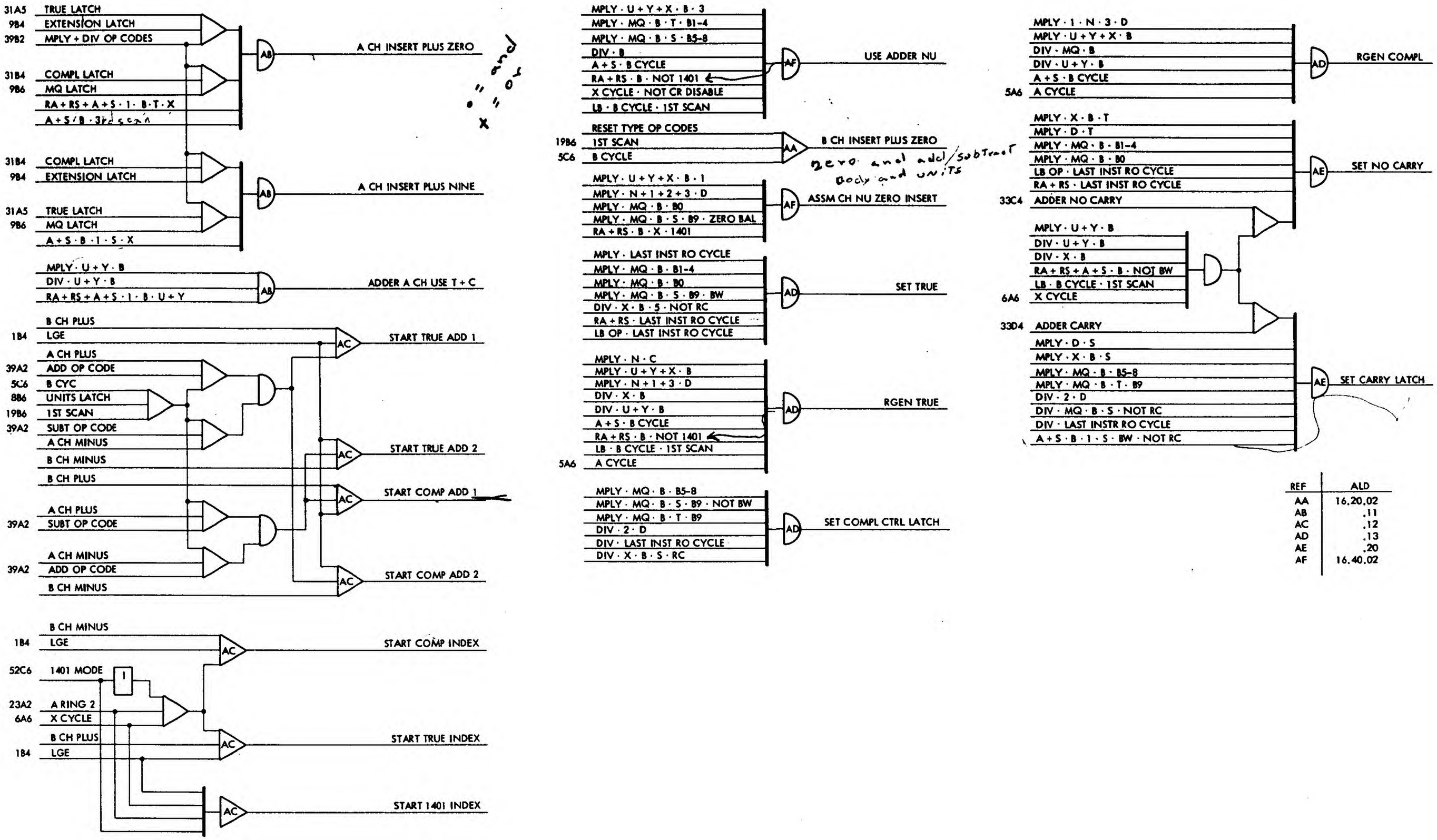


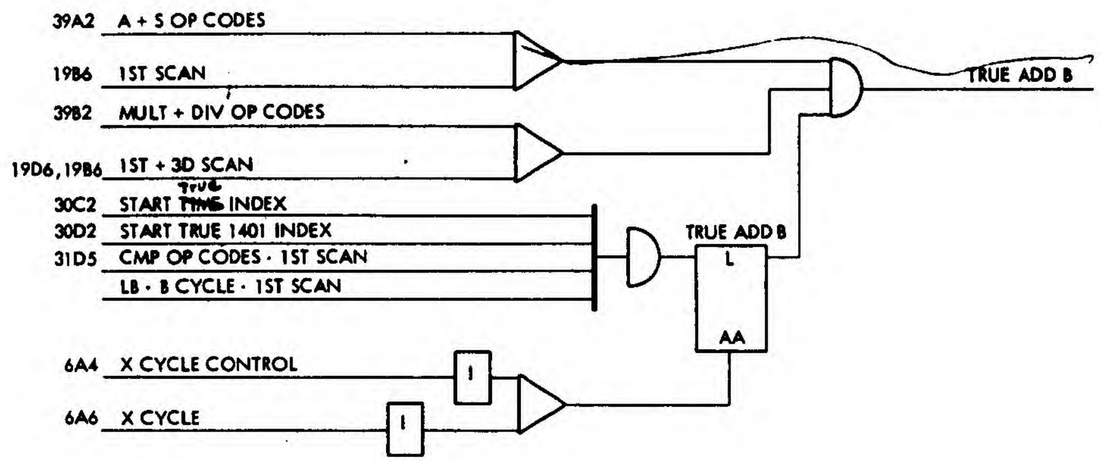
FIGURE 29. ASSM CHAN 1,2,4,8,A AND B BITS

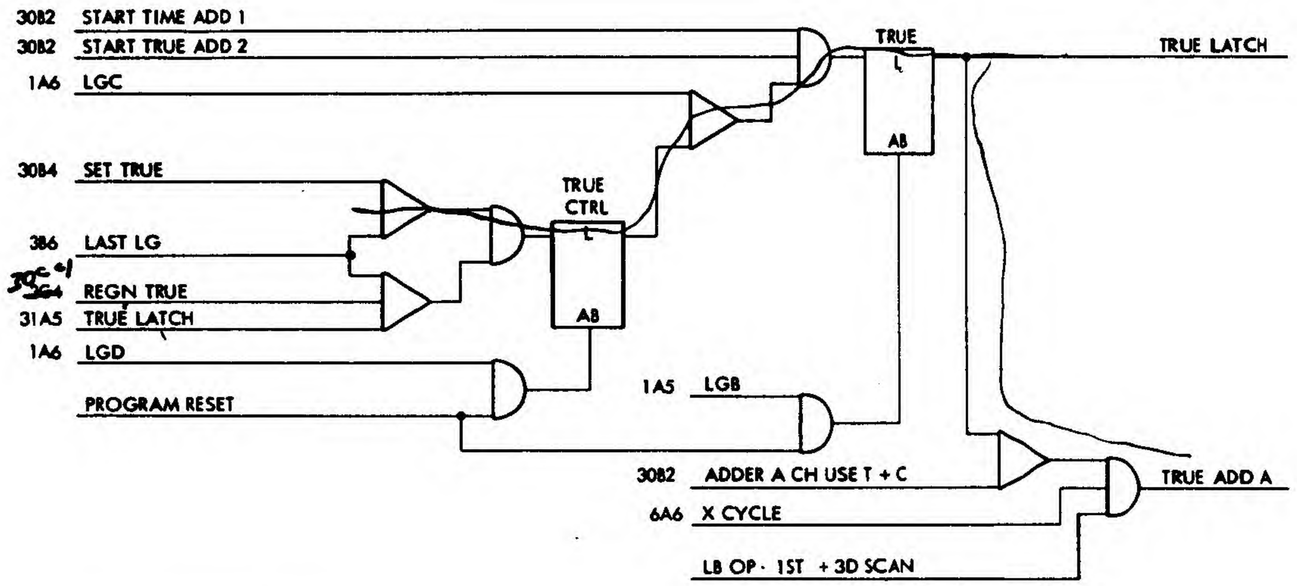
T = True add

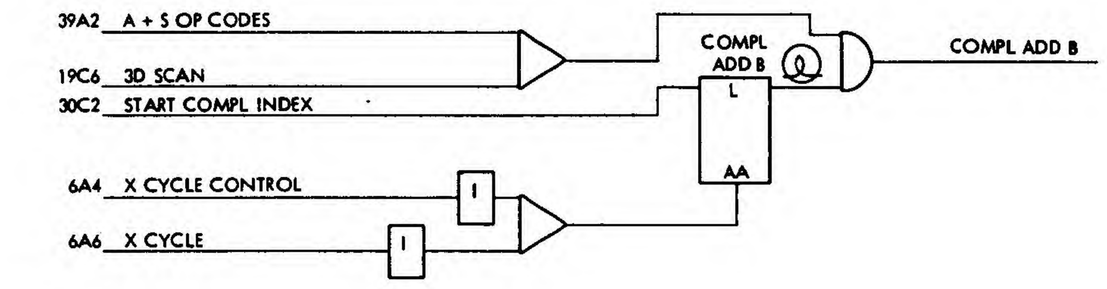


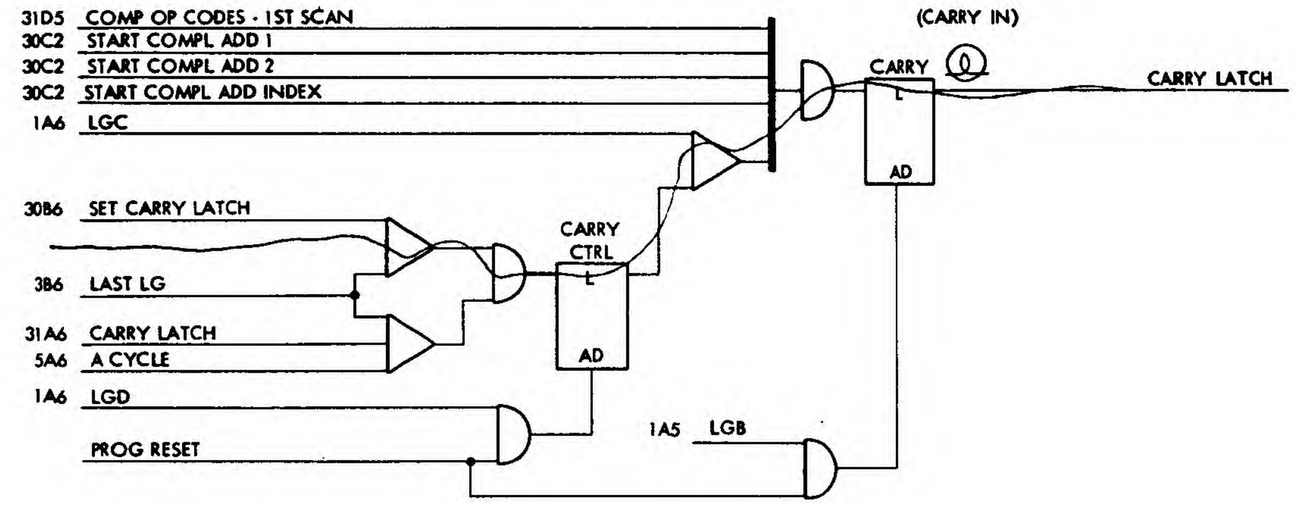
REF	ALD
AA	16.20.02
AB	.11
AC	.12
AD	.13
AE	.20
AF	16.40.02

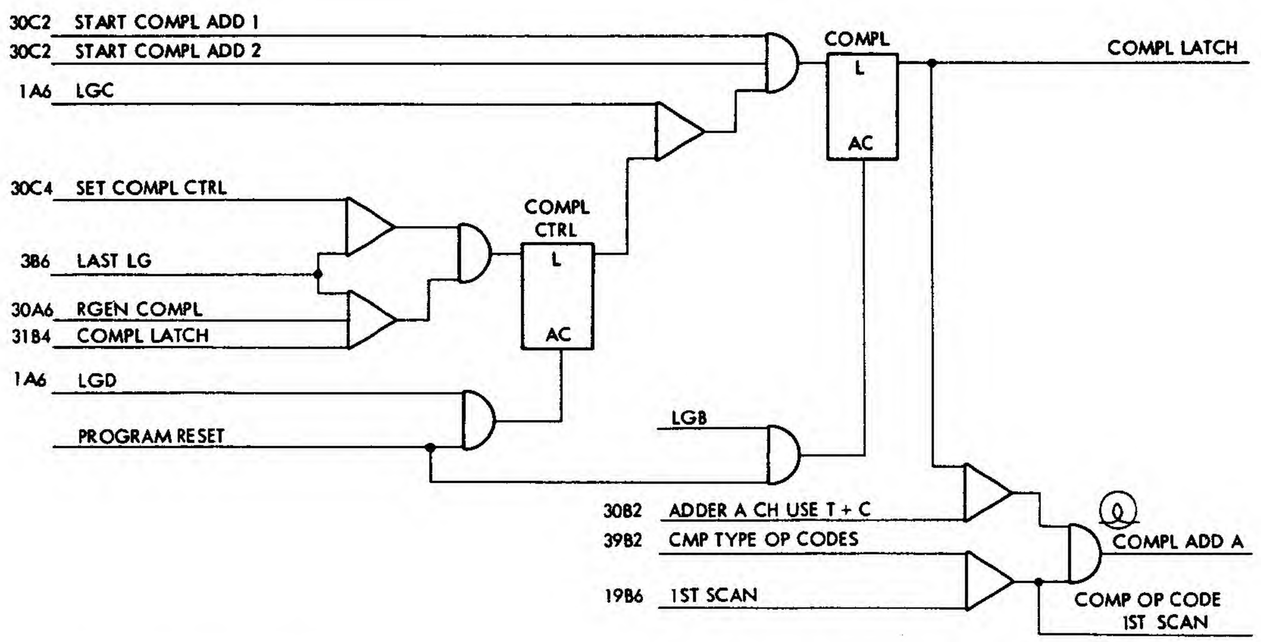
FIGURE 30. ADDER CTRL LINES

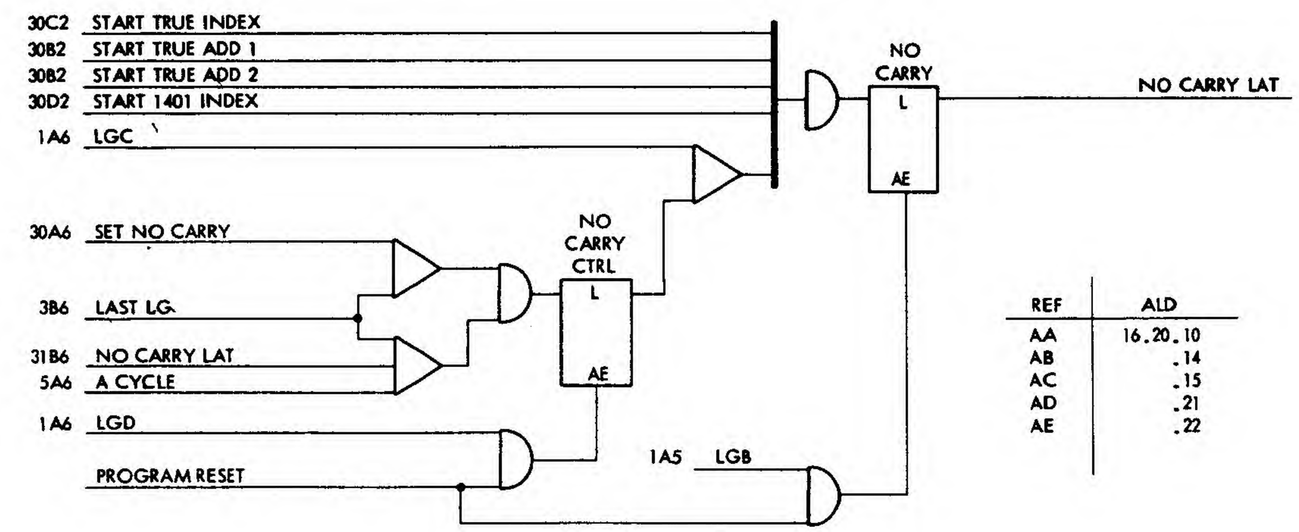












REF	ALD
AA	16.20.10
AB	.14
AC	.15
AD	.21
AE	.22

FIGURE 31. ADDER CTRL LATCHES

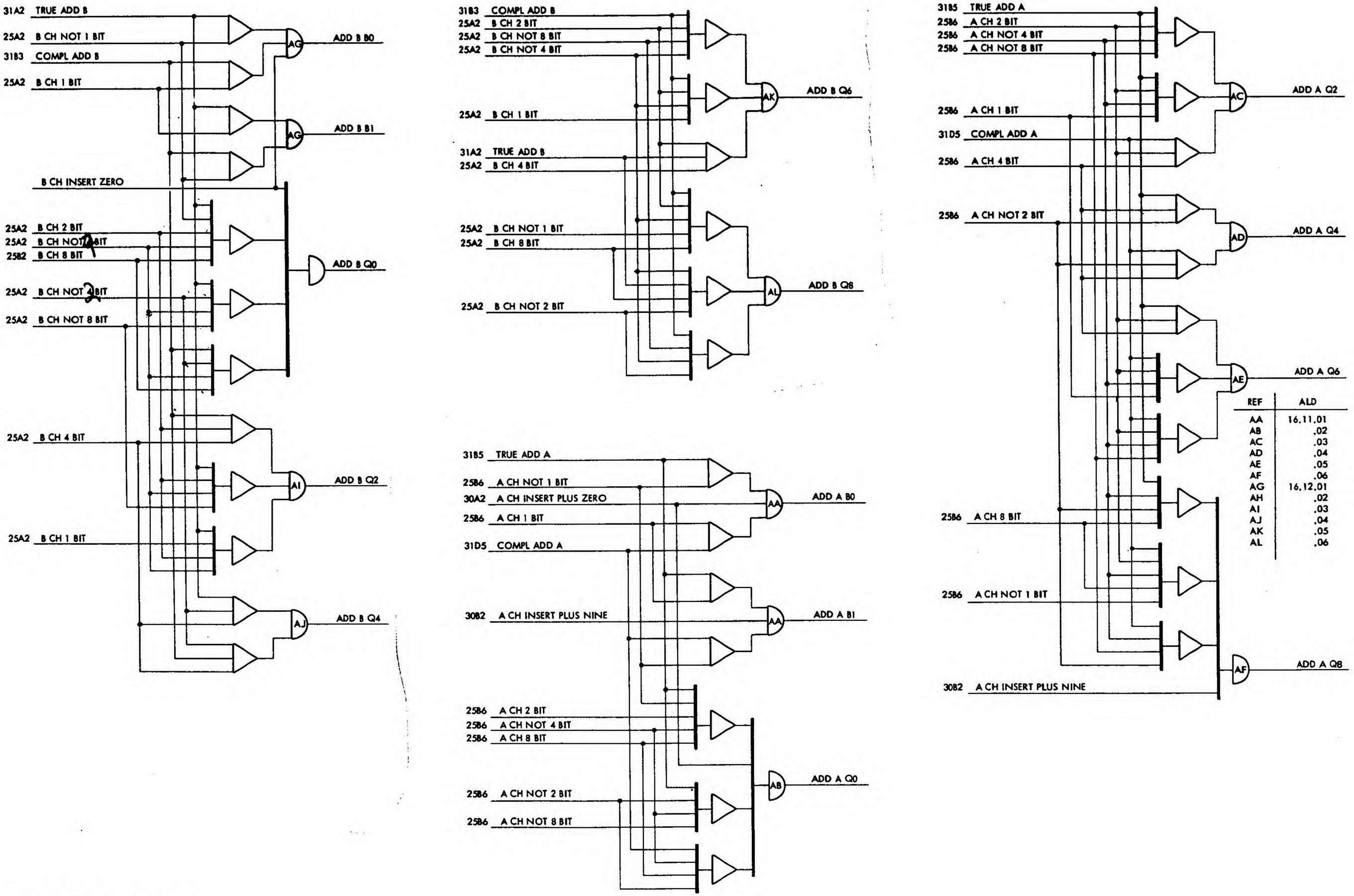
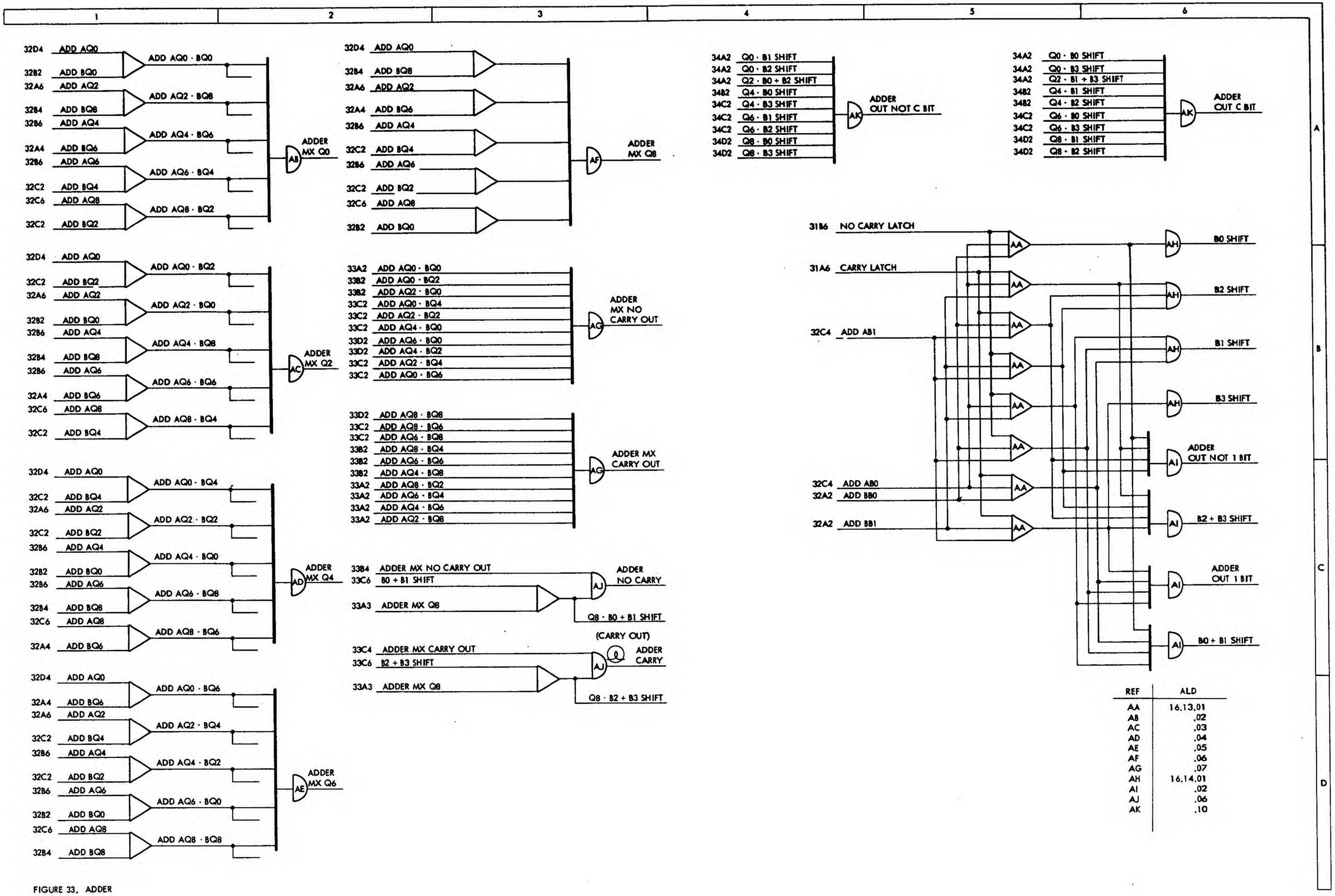
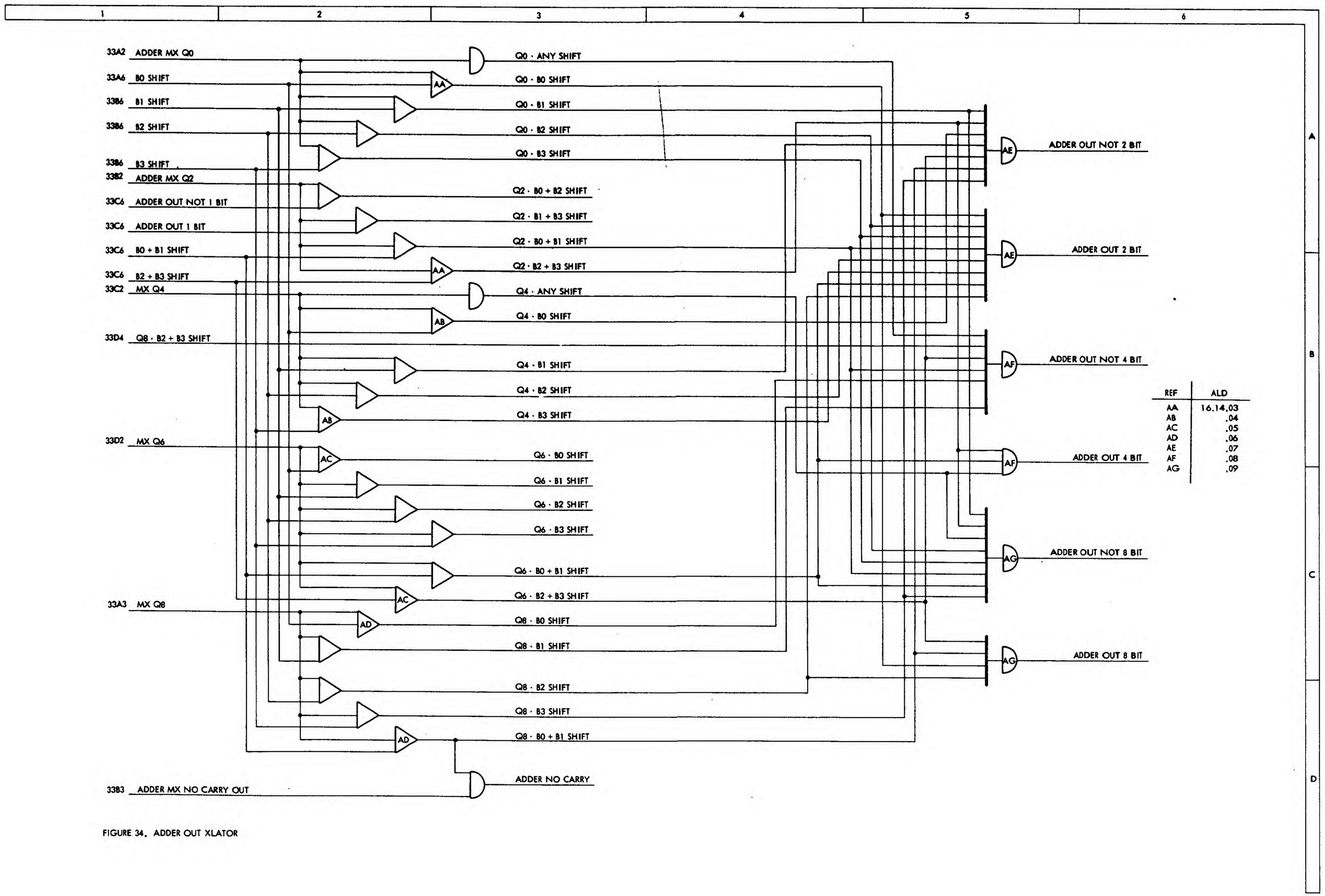


FIGURE 32. ADDER BCD TO QUI-BINARY



REF	ALD
AA	16.13.01
AB	.02
AC	.03
AD	.04
AE	.05
AF	.06
AG	.07
AH	16.14.01
AI	.02
AJ	.06
AK	.10

FIGURE 33. ADDER



REF	ALD
AA	16.14.03
AB	.04
AC	.05
AD	.06
AE	.07
AF	.08
AG	.09

FIGURE 34. ADDER OUT XLATOR

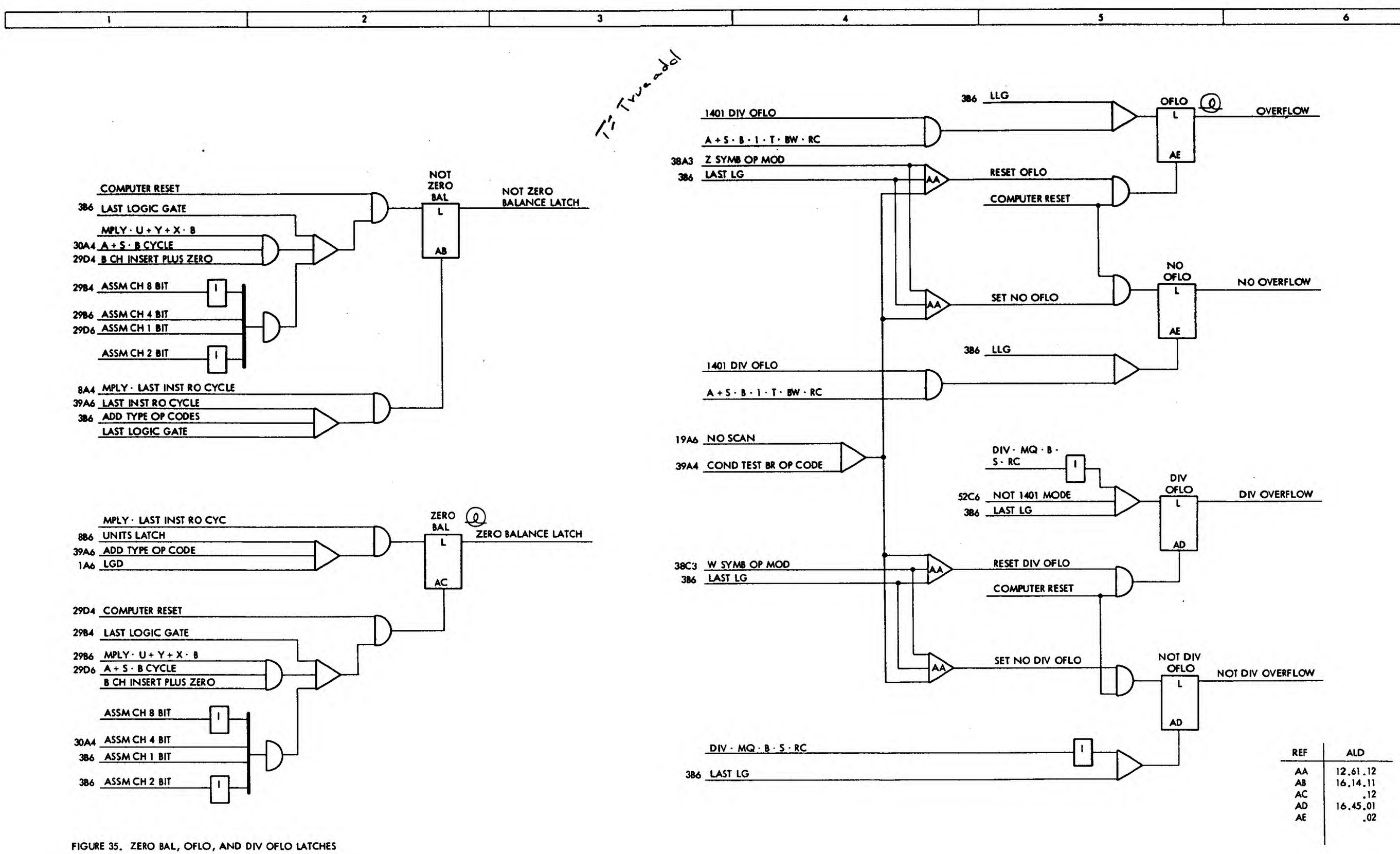


FIGURE 35. ZERO BAL, OFLO, AND DIV OFLO LATCHES

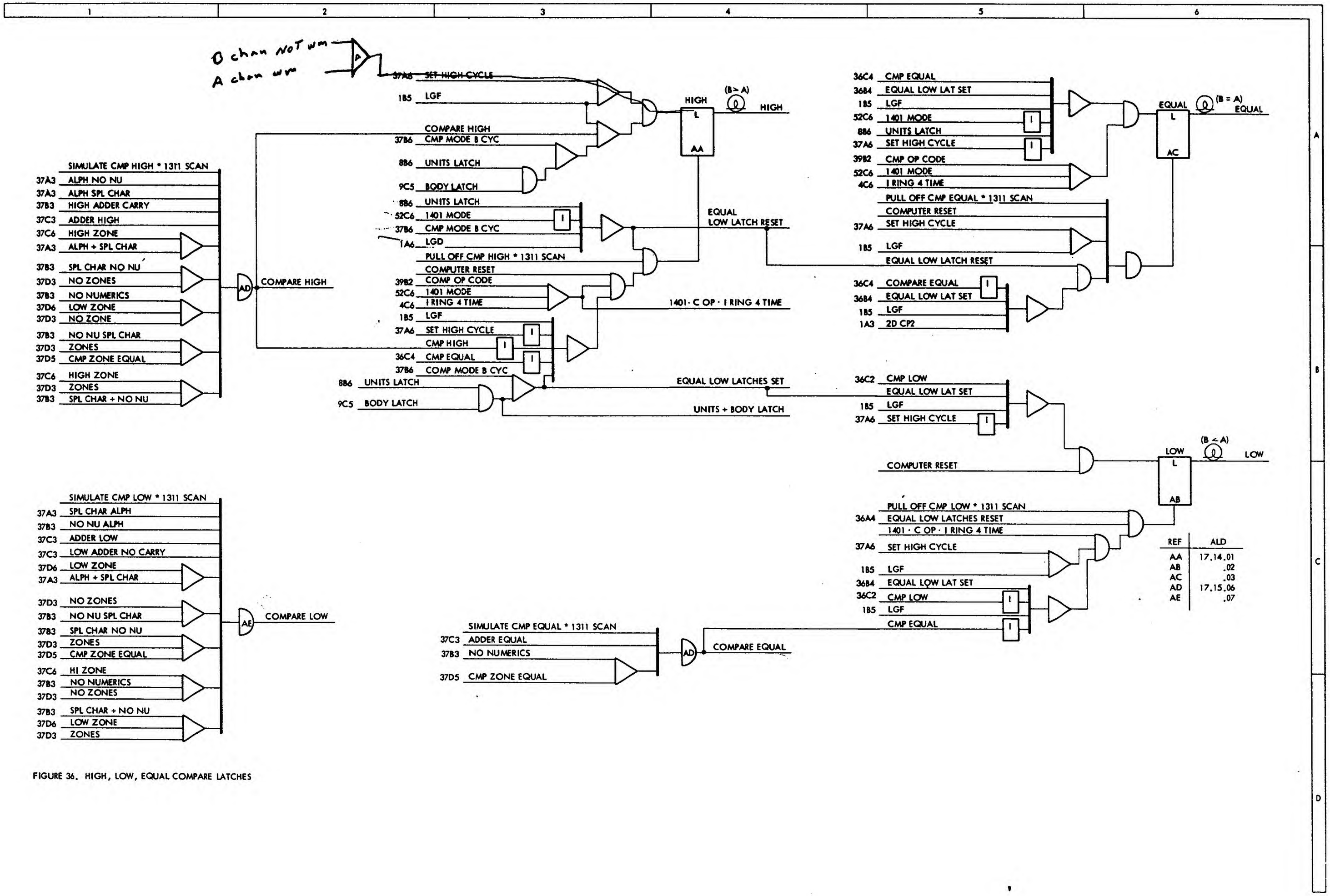


FIGURE 36. HIGH, LOW, EQUAL COMPARE LATCHES

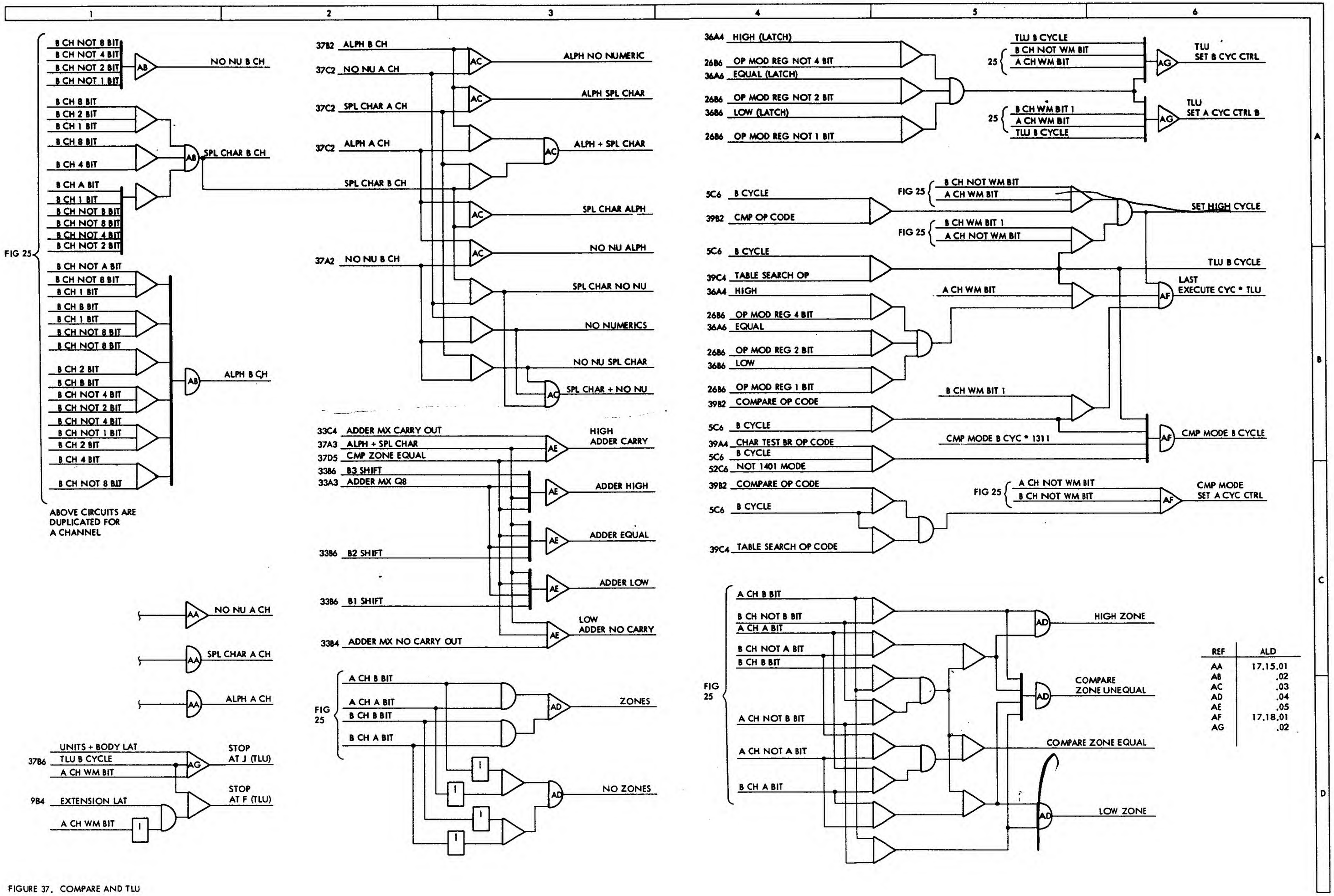
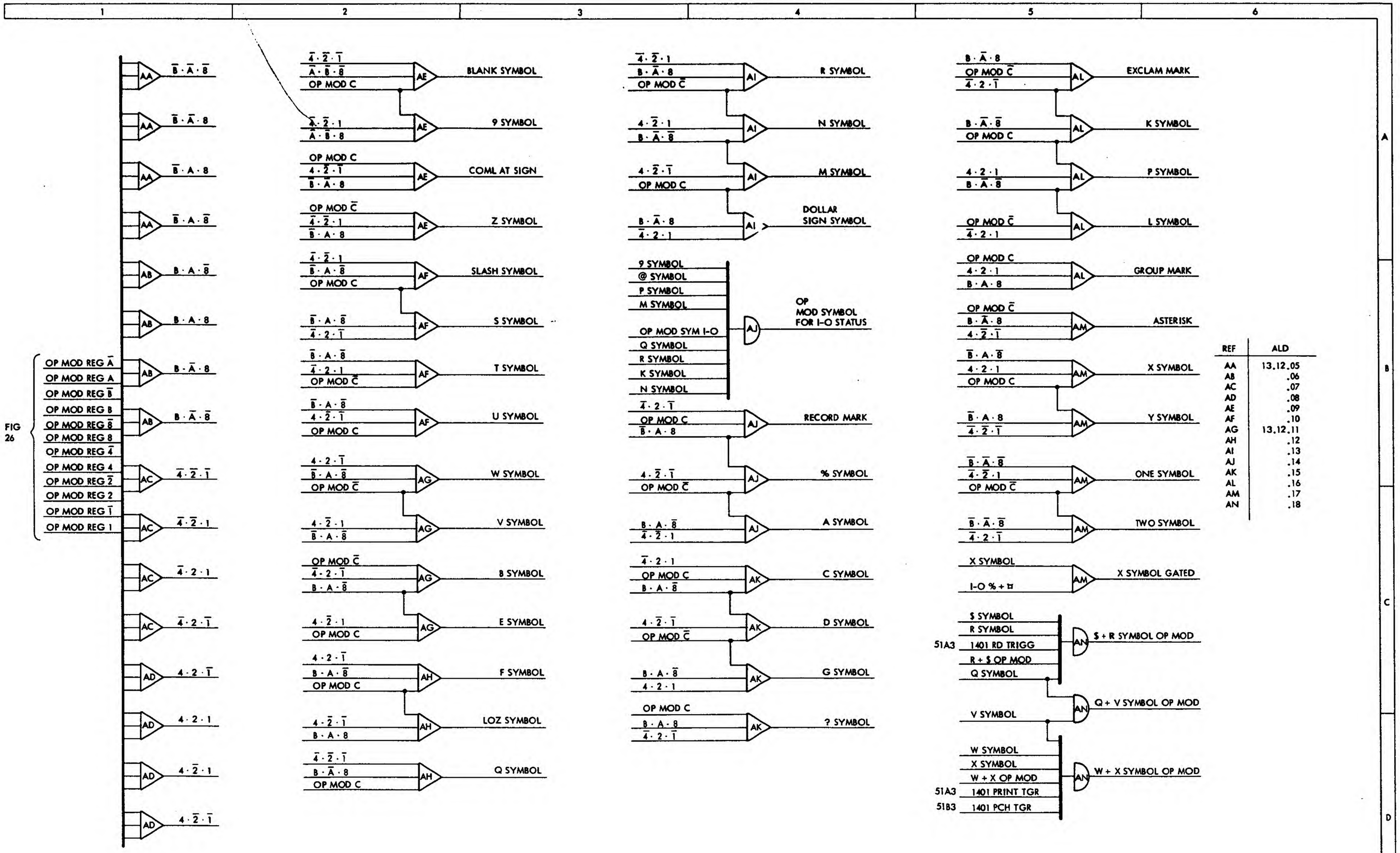


FIGURE 37. COMPARE AND TLU



REF	ALD
AA	13.12.05
AB	.06
AC	.07
AD	.08
AE	.09
AF	.10
AG	13.12.11
AH	.12
AI	.13
AJ	.14
AK	.15
AL	.16
AM	.17
AN	.18

FIGURE 38. OP MOD DECODE

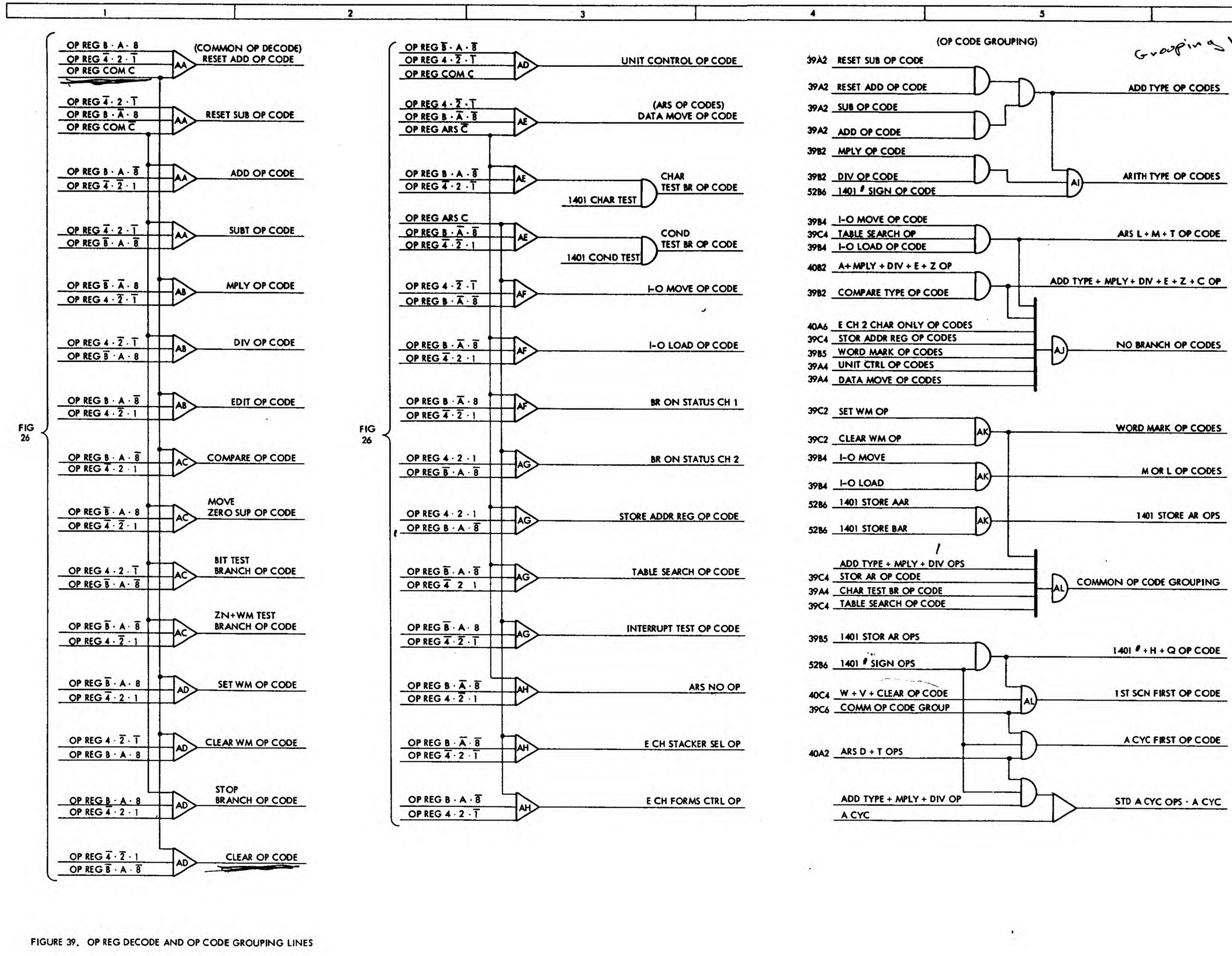


FIGURE 39. OP REG DECODE AND OP CODE GROUPING LINES

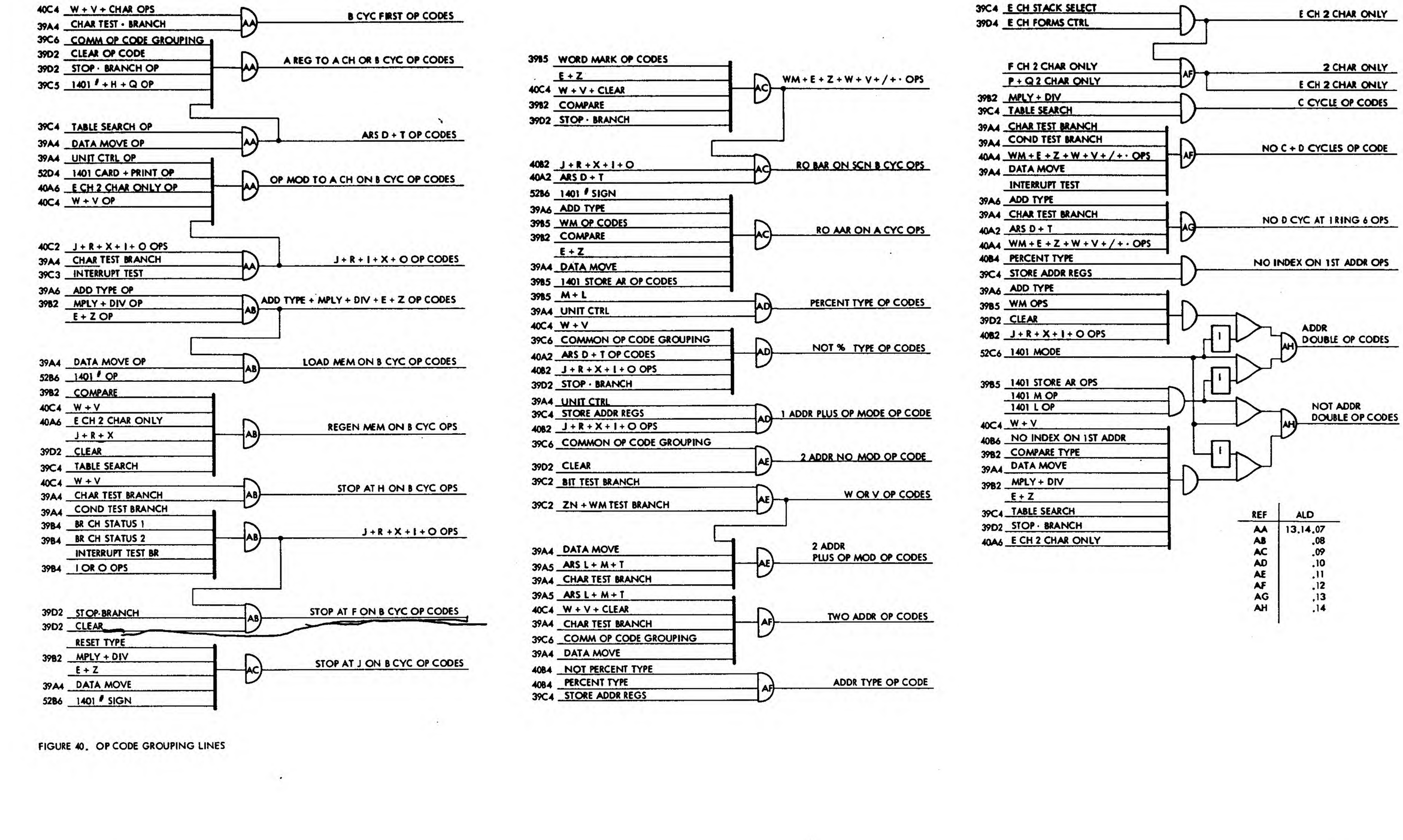


FIGURE 40. OP CODE GROUPING LINES

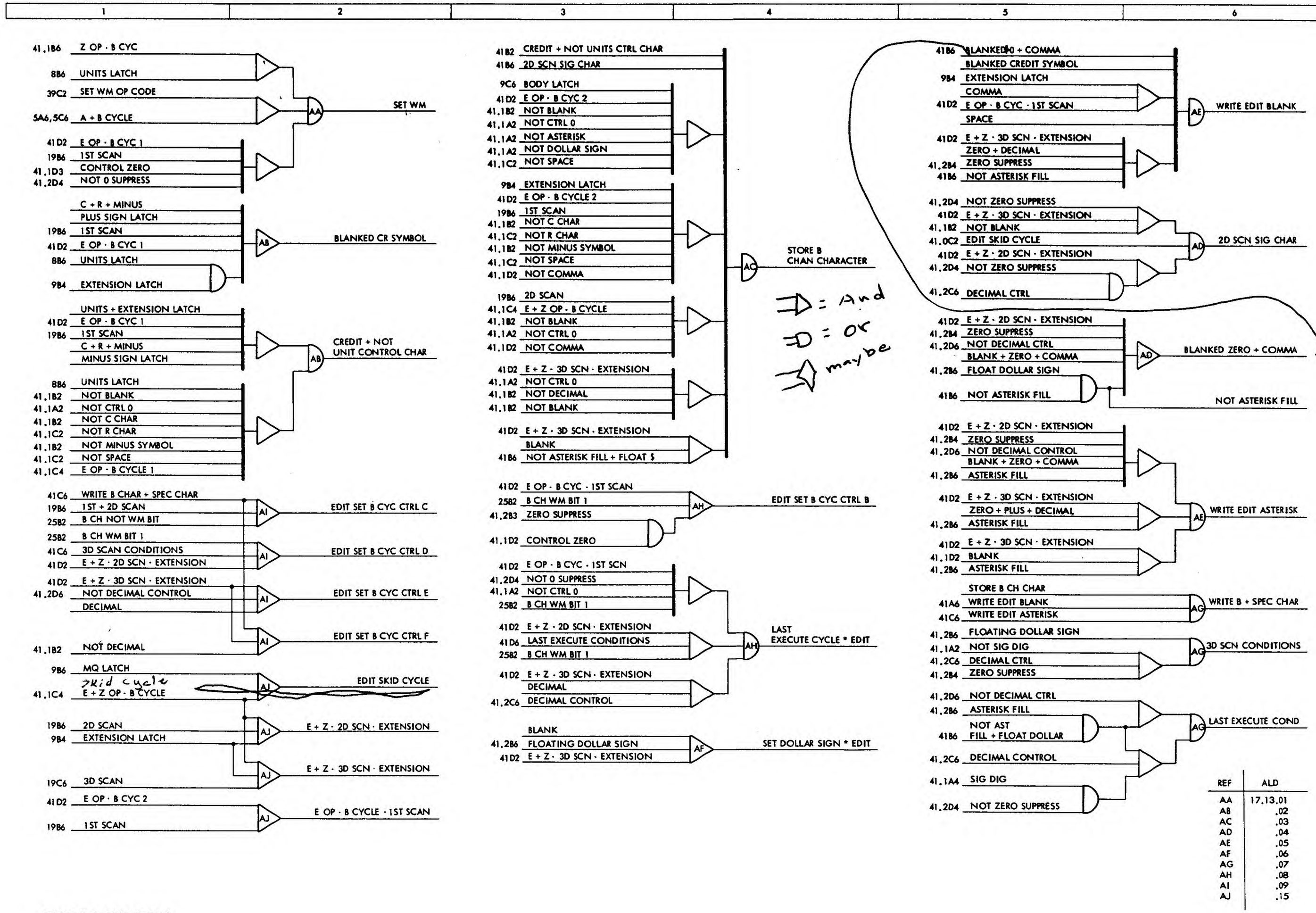
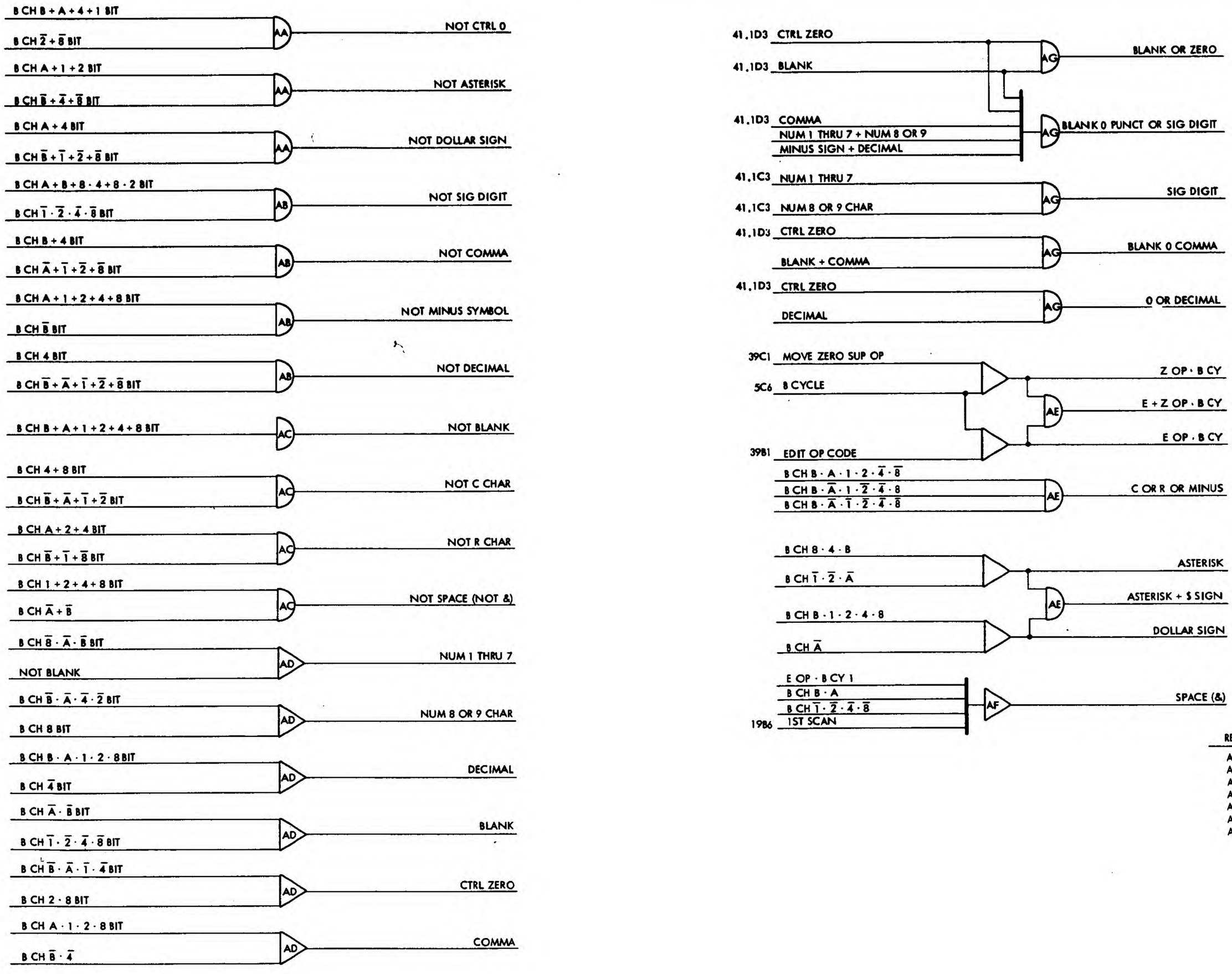


FIGURE 41.0 EDIT CONTROL



REF	ALD
AA	17.11.01
AB	17.11.02
AC	17.11.03
AD	17.11.05
AE	17.11.04
AF	17.11.07
AG	17.11.06

FIGURE 41.1 EDIT TRANSL

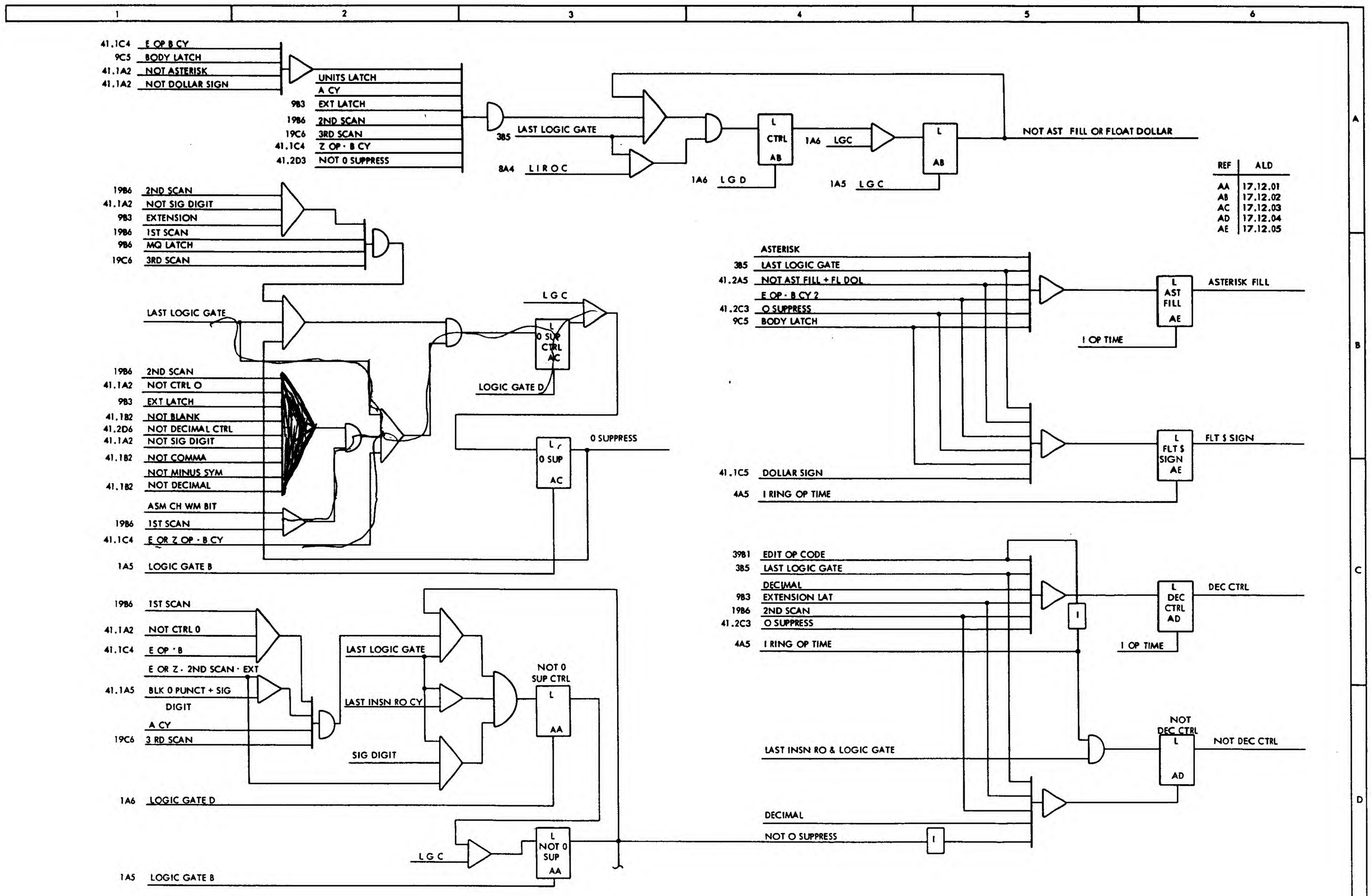


FIGURE 41.2. EDIT LATCHES

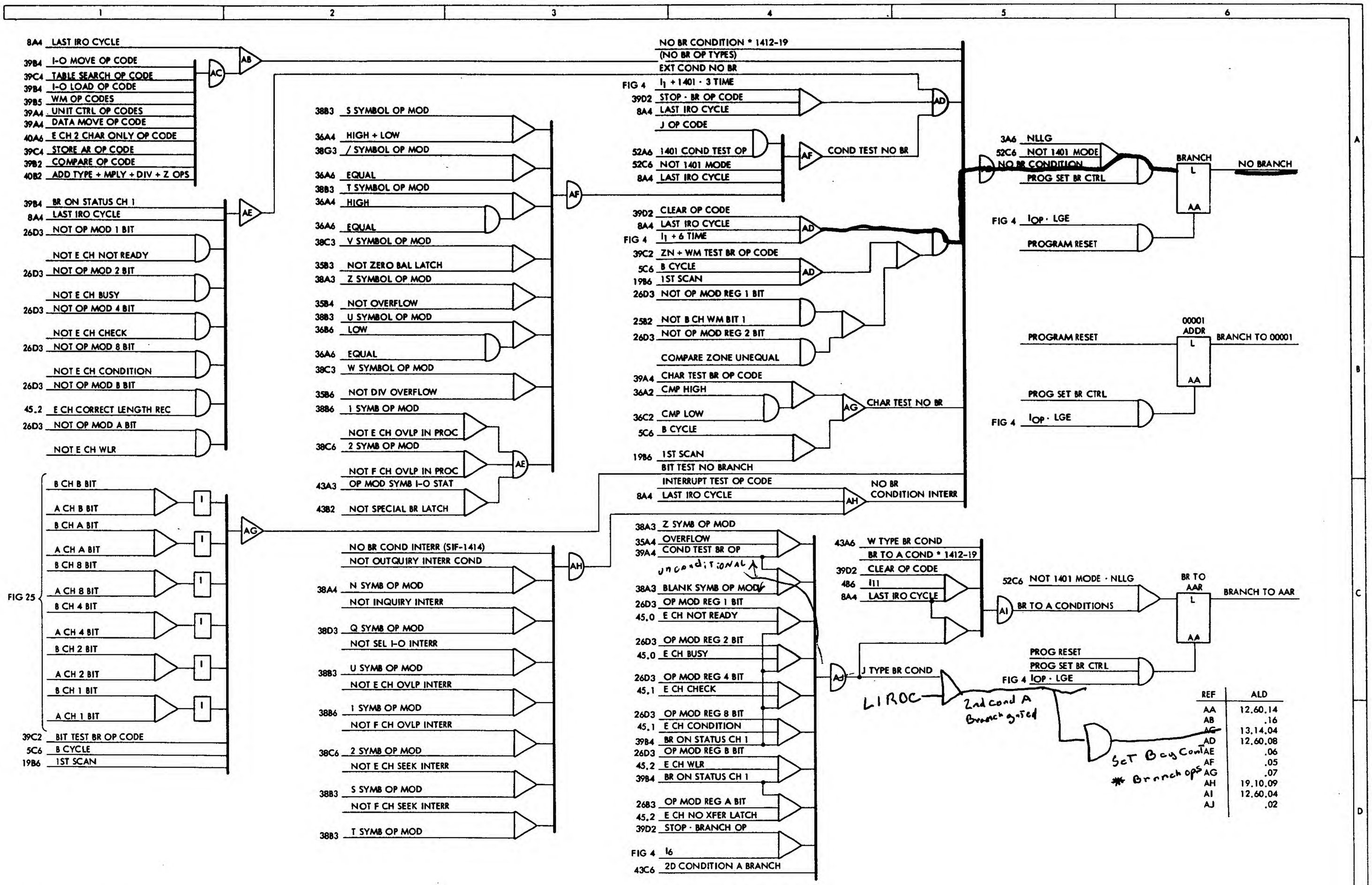


FIGURE 42. BRANCH - NO BRANCH I

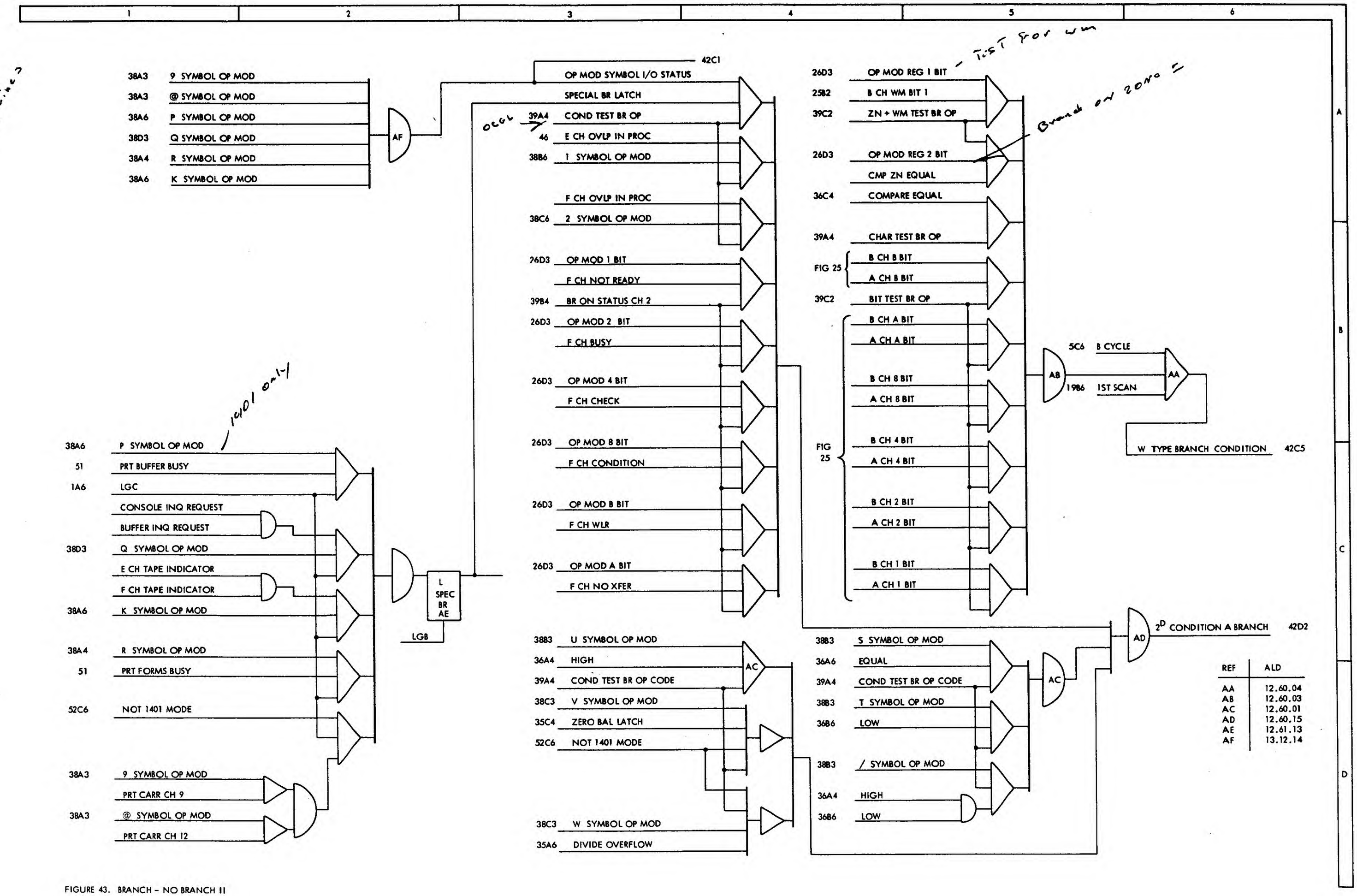


FIGURE 43. BRANCH - NO BRANCH II

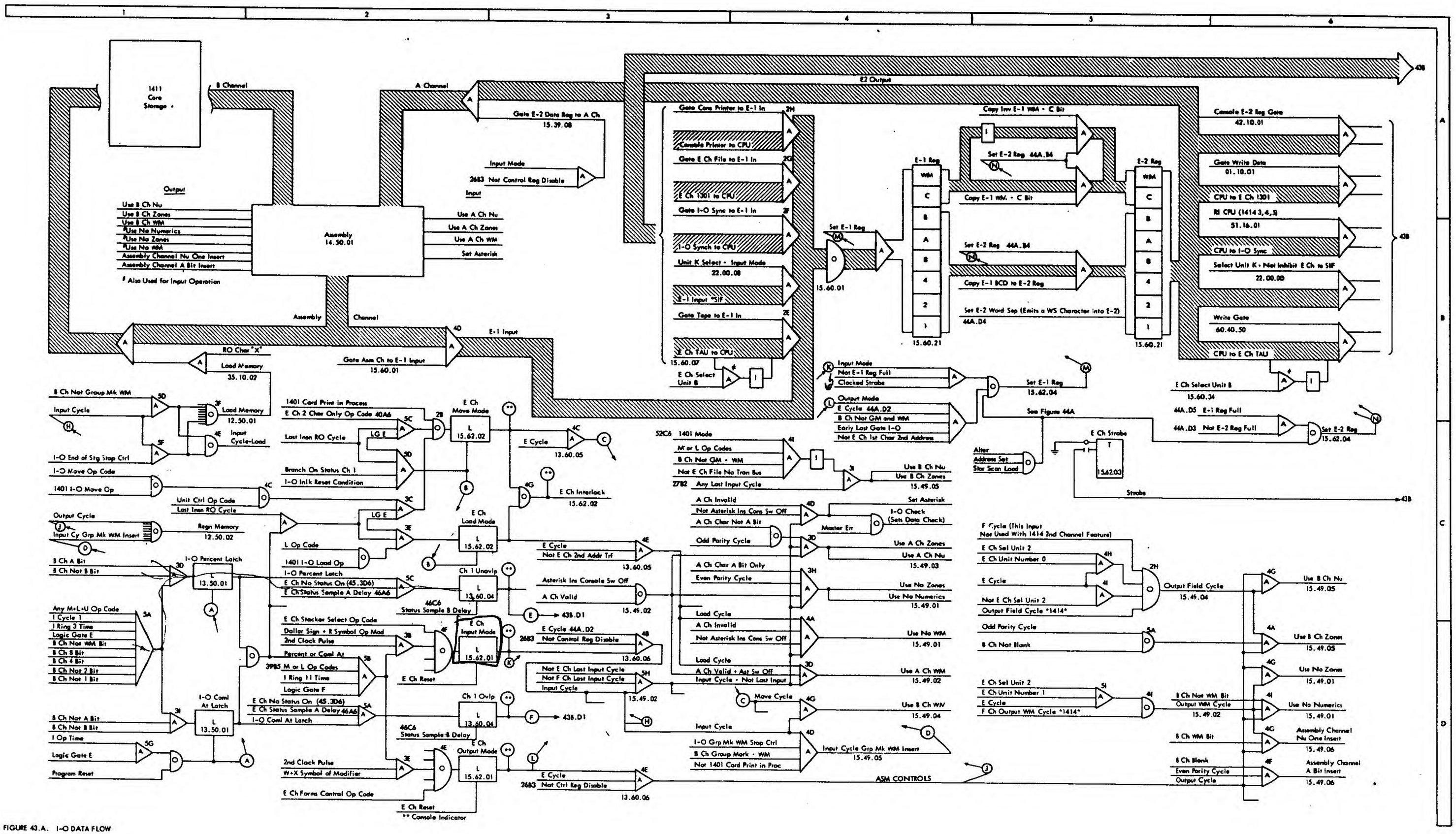


FIGURE 43.A. I-O DATA FLOW

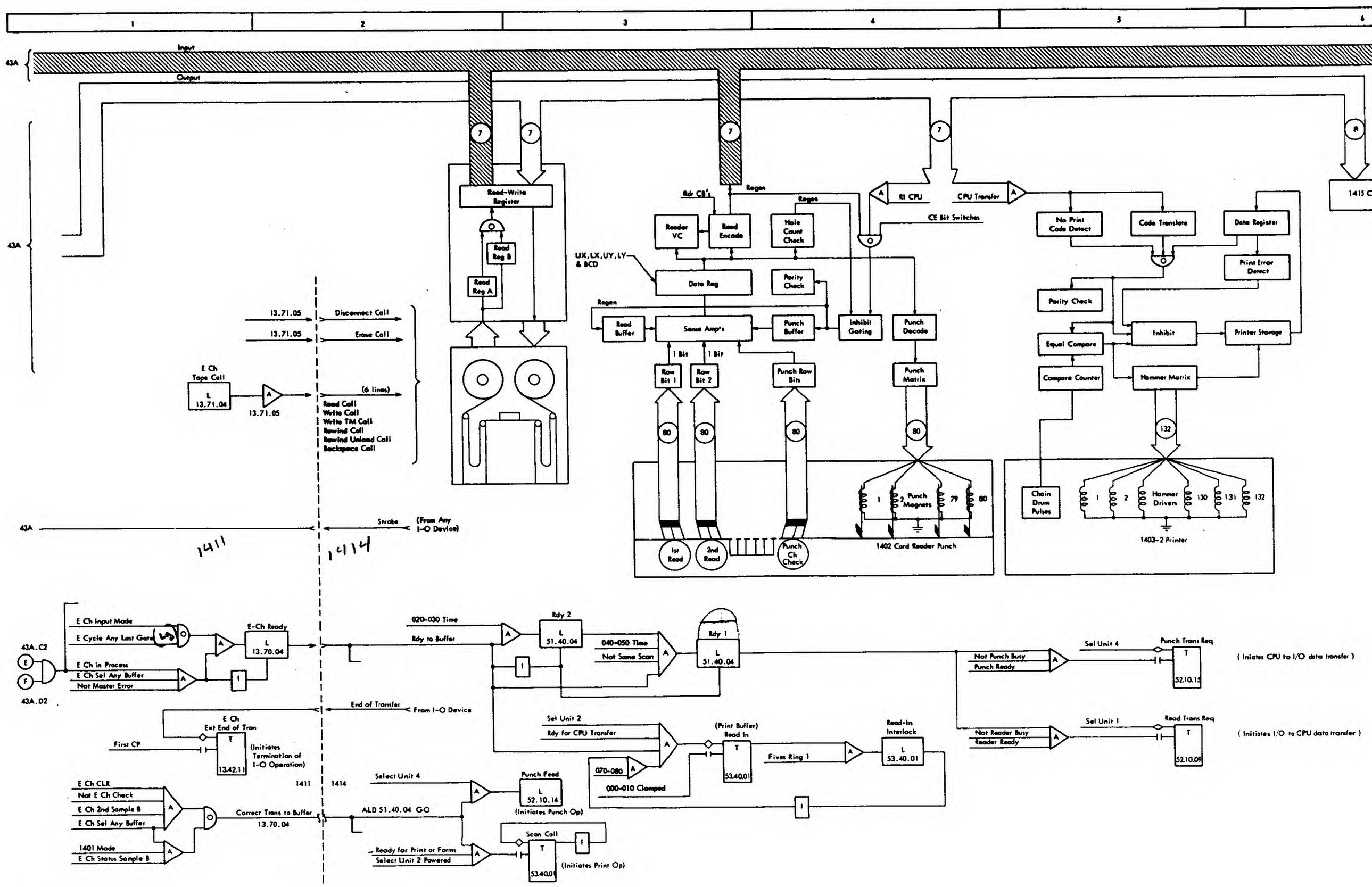


FIGURE 43.8. I-O DATA FLOW

See Page 1-1414 I/O

A | B | C | D

1414 | 1411

Strobe
L
51.40.43
I-O to CPU Transfer
Time 080-090

51.40.11
Input Data Lines From 1414-3, 4, or 5
Input Mode
E-CH Select Any Buffer

E-Channel Strobe
Buffer Strobe
E-CH Sel Any Buffer
Set E-1 Reg
Input Mode
43A.C3
T ** 15.62.03
On
(Pulls Trigger Off)

E-Channel Clocked Strobe
2nd CP
T ** 15.62.03
On
(Pulls Trigger Off)

Set E-1 Reg
1st CP
2nd CP
T ** 15.62.04
On
Off
SET E1 REG PULSE

Clocked Strobe
Not E-1 Reg Full
Input Mode
(Holds Trigger Off)

E-1 Reg Full
L** 15.41.10

E-1 Data Reg one-bit 15.60.21

E-CH Wd Sep Mode
E-CH Wd Sep
E-1 Input WM Bit
E-1 Reg Wd Sep
L** 15.41.11

39B5 M or L OP Codes
43A.C2 Percent or Comi At
45 Select Unit 1 or Unit 4
4D5 I Cycle
4B5 I Ring 5 Time
2B4 LG Early B or S

Places Stacker Character On E Channel

Not E-CH Wd Sep
Not E-1 Input WM Bit

The Three Copy Control Lines Are Not Shown
1. Copy E-1 BCD to E-2 Reg
2. Copy E-1 WM C Bit
3. Copy Invert E-1 WM C Bit 15.62.06

E-1 Reg Word Sep
Not E-2 Reg Word Sep
Not Gate Cons to Asm
E-CH Input Mode
Not E-1 Reg Wd Sep
E-2 Reg Wd Sep

Set E-2 Reg
1st CP
2nd CP
T ** 15.62.04
On
Off
(Holds Trigger Off)

Set E-2 Wd Sep

E-2 Data Reg One-Bit 15.60.21

E-2 Reg Full
L** 15.41.10

E-1 Full
Not E-2 Full

Reset E-2 Full Latch
1st CP
2nd CP
T ** 15.62.05
On
Off
(Holds Trigger Off)

15.39.01
Input Mode
E-Cycle
To A-Channel

E Cycle
Input Cycle Not Last Input 43A
Input Cycle Load
Early Last I-O Gate
43A Input Cycle
B-CH Not GM-WM
T6 RDR Only

Set E-2 Reg Delayed
1st CP
T ** 15.62.04
On

E-1 Reg Wd Sep
E-CH Wd Sep Mode
E-2 Reg Wd Sep
L** 15.41.11

Reset E-2 Full Latch
E-CH Input Mode 43A

* Collector Pullover
** E-Channel Reset

Console Indicator

E-CH in Process 43B.C1
E-CH Input Mode 43A.D3
E-2 Reg Full
Not E-CH Int End of Tran 46B5
Not E Cycle and Any Last Gate
E Cycle Required 12.12.62

Not F Cycle Required
Not E Channel Int End of Tran
Logic Gate Z
2nd Clock Pulse
Z

E Cycle Control
L 12.12.66
Logic Gate D or U

Logic Gate B or S
E Cycle
L 12.12.66

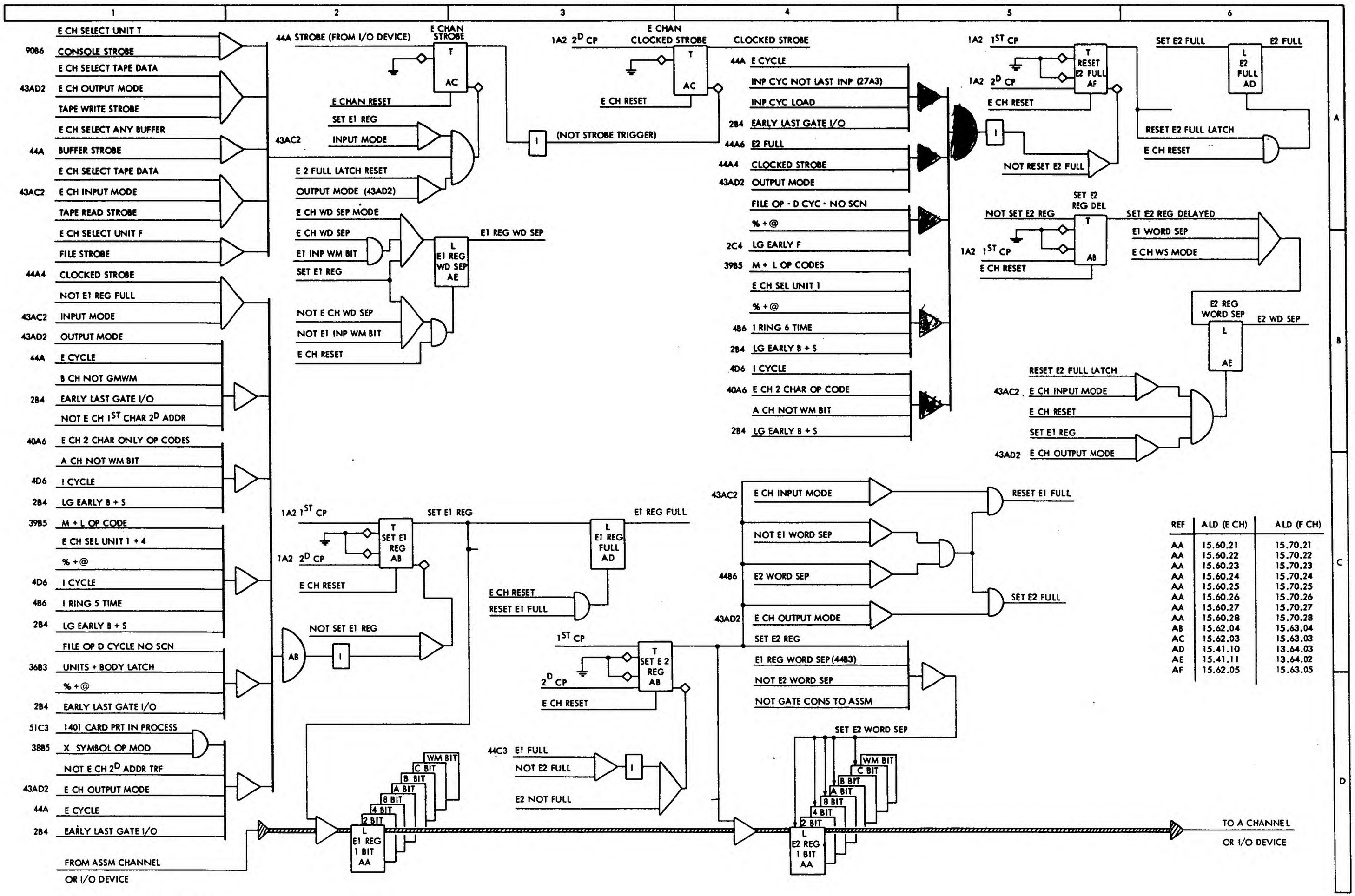
E-CH Unoverlap in Process
E-CH 2nd Address Unoverlap
Not Console Inhibit AR Read Out
Not 1st I-O Cycle Control (1401)
E Cycle Control
Read Out BAR 14.71.31

Logic Gate Early B
1st Clock Pulse
Reset Bar 14.71.21

Logic Gate B or C
E Cycle And Logic Gate D or E or F
Set Bar 14.71.11

E-Ch Input Mode 43A
E-Ch In Process 43B
E-Ch Sel Any Buffer
Not Master Error
E-Ch Ready
L 13.70.04
Rdy To Buffer

FIGURE 44A. E CHANNEL REG AND CONTROLS (RDR)



REF	ALD (E CH)	ALD (F CH)
AA	15.60.21	15.70.21
AA	15.60.22	15.70.22
AA	15.60.23	15.70.23
AA	15.60.24	15.70.24
AA	15.60.25	15.70.25
AA	15.60.26	15.70.26
AA	15.60.27	15.70.27
AA	15.60.28	15.70.28
AB	15.62.04	15.63.04
AC	15.62.03	15.63.03
AD	15.41.10	13.64.03
AE	15.41.11	13.64.02
AF	15.62.05	15.63.05

FIGURE 44. E & F CHAN REG & CTRL

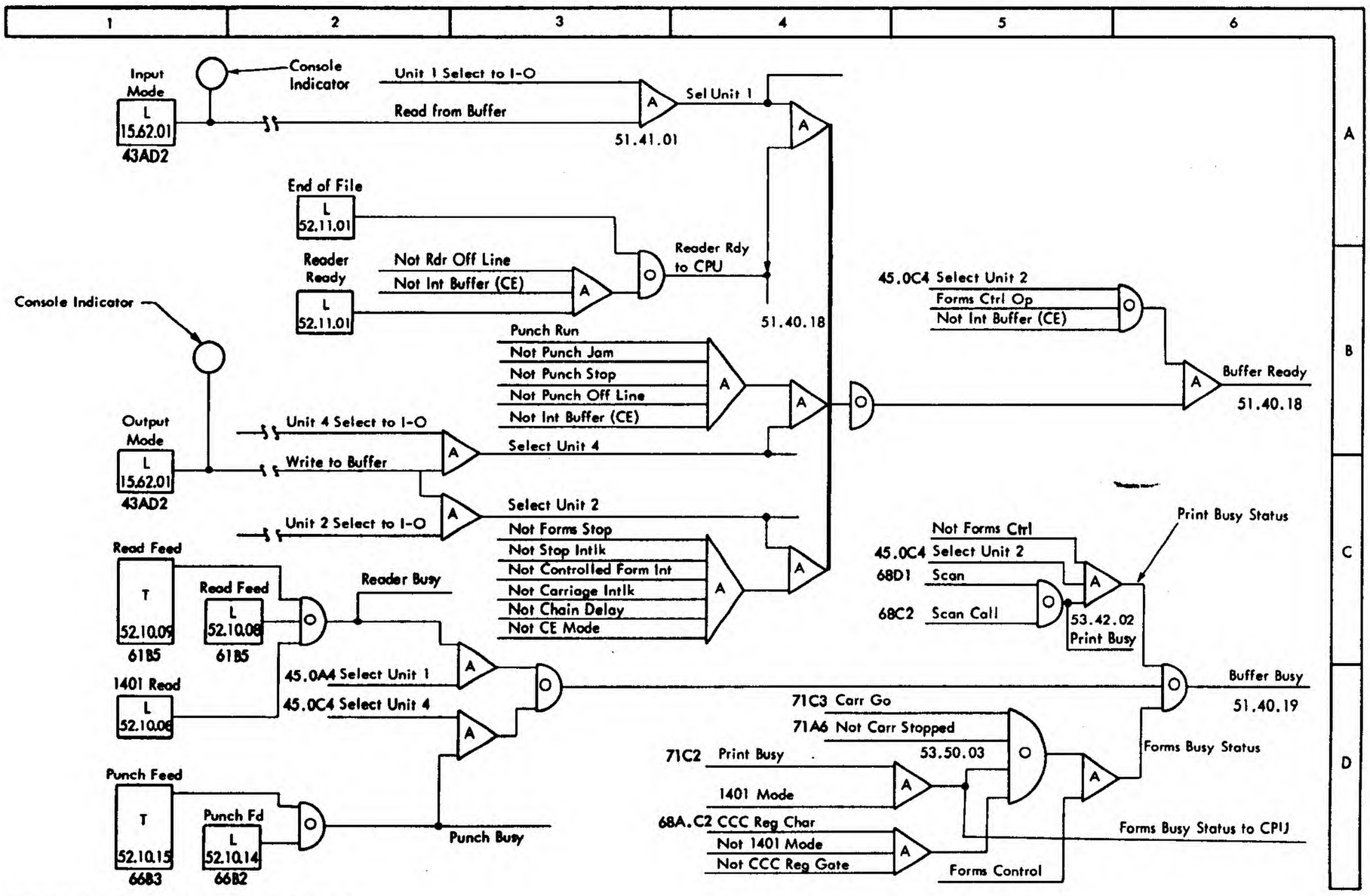


FIGURE 45.0. CHANNEL NOT READY OR BUSY

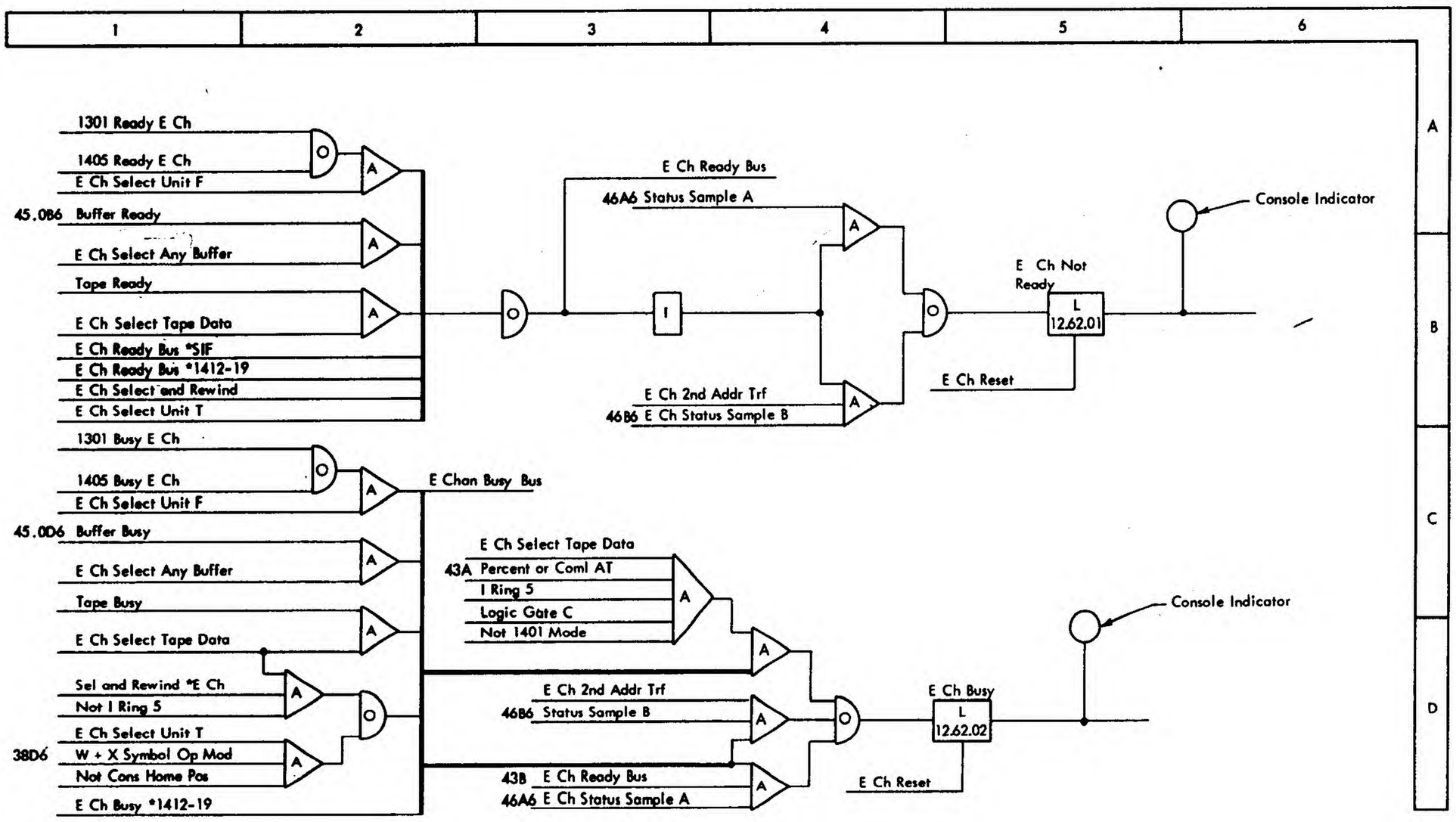


FIGURE 45.1. CHANNEL NOT READY OR BUSY

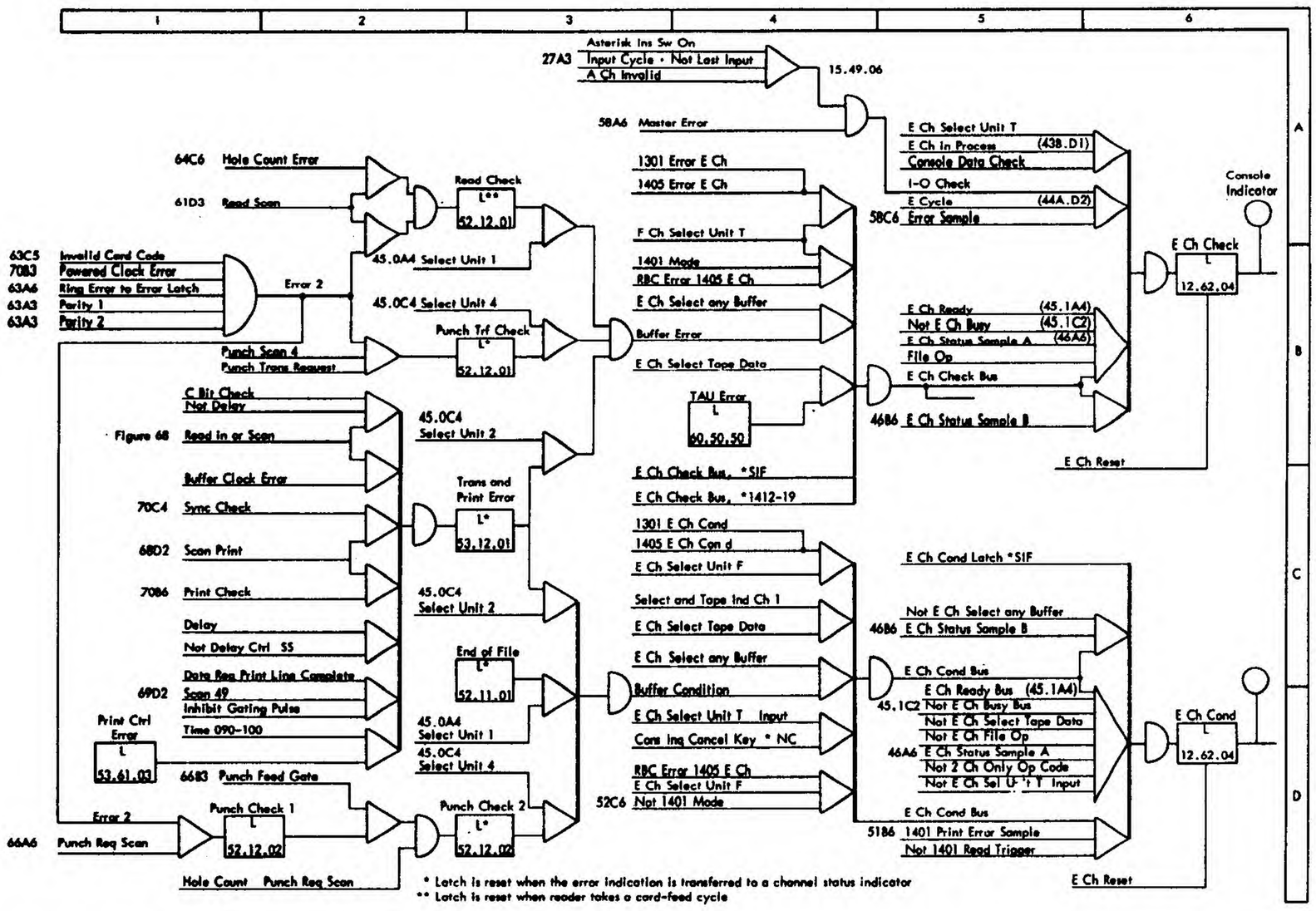


FIGURE 45.2. E CHAN CHECK AND COND

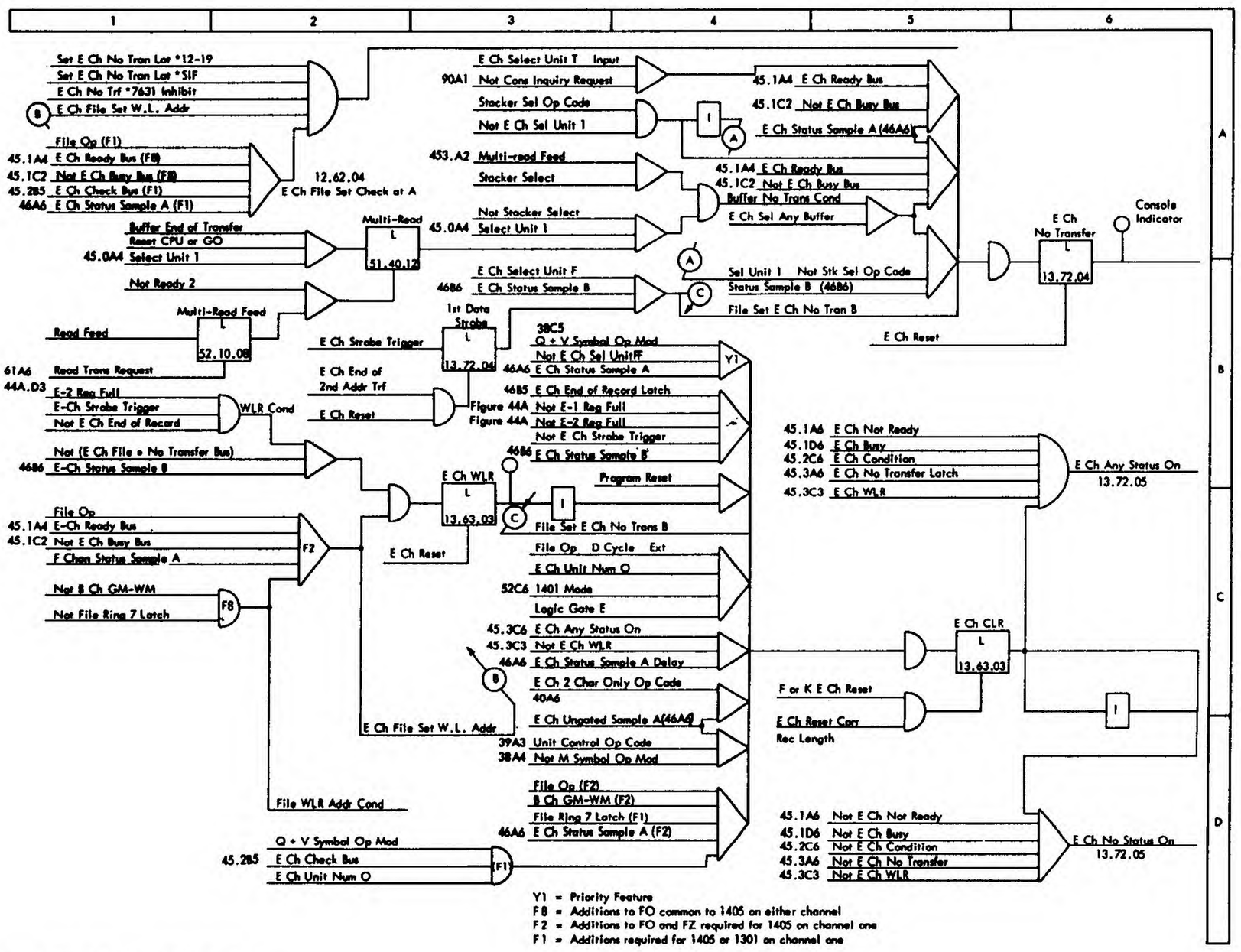


FIGURE 45.3. E CHANNEL WLR AND NO TRF

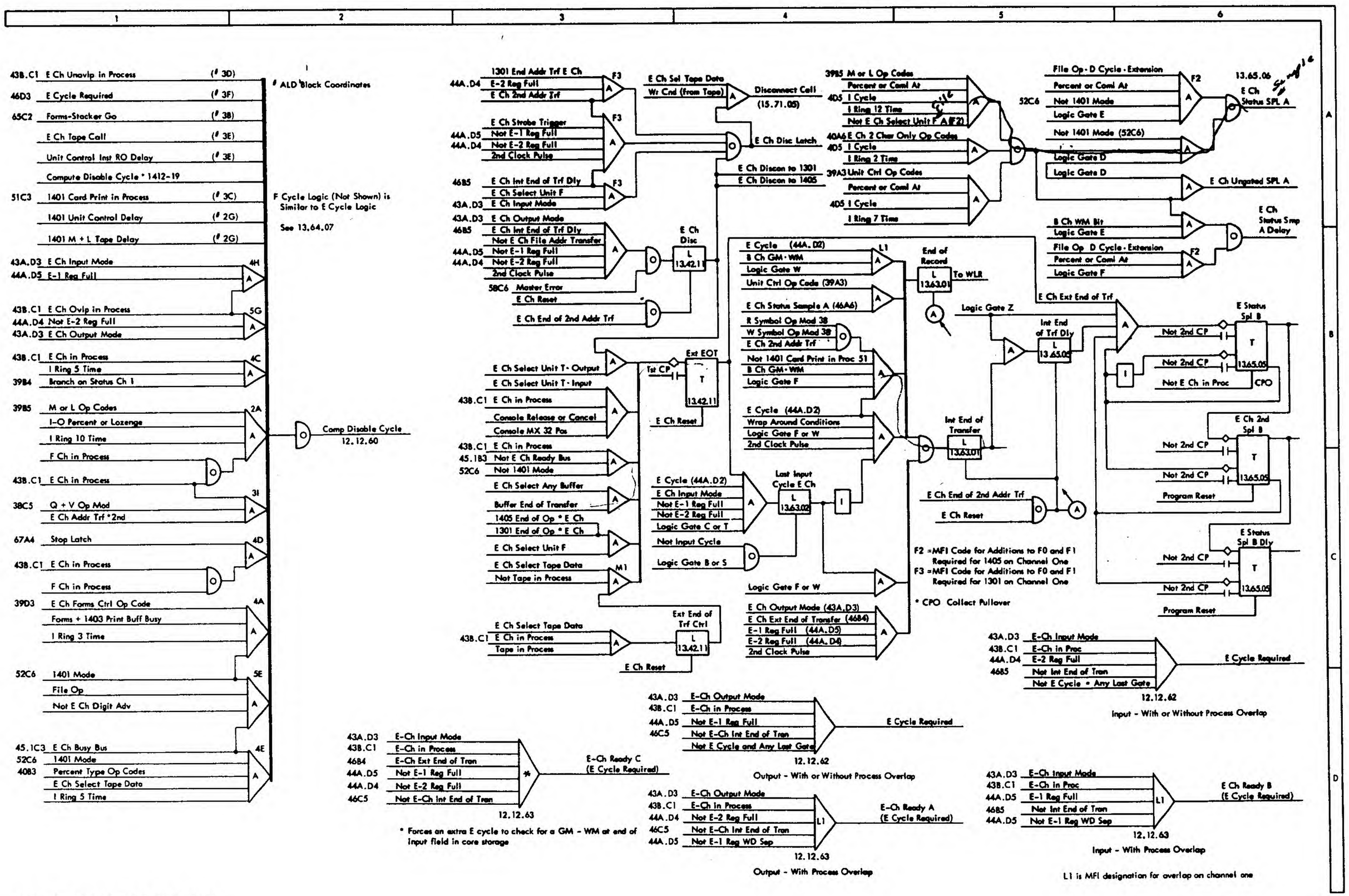
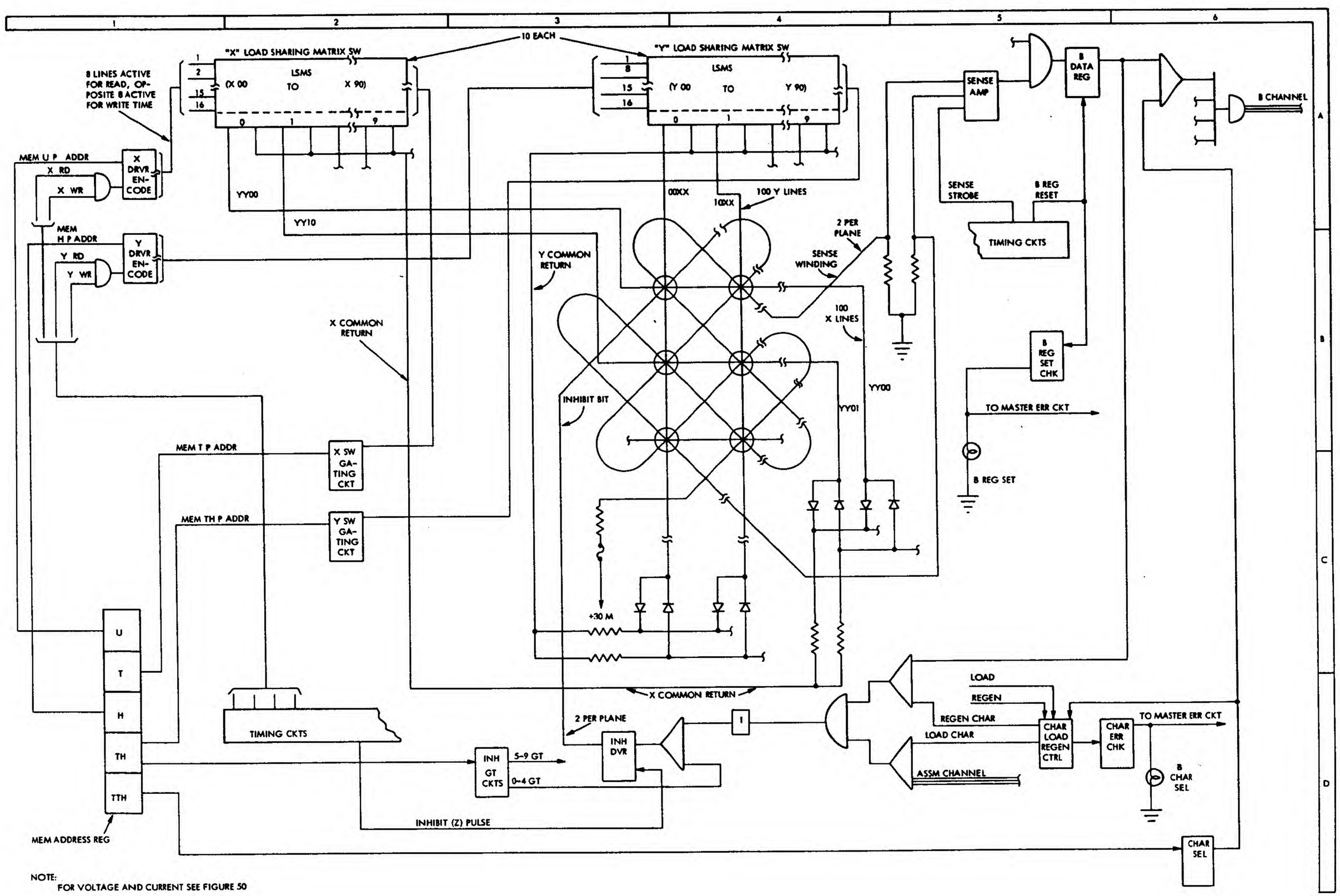
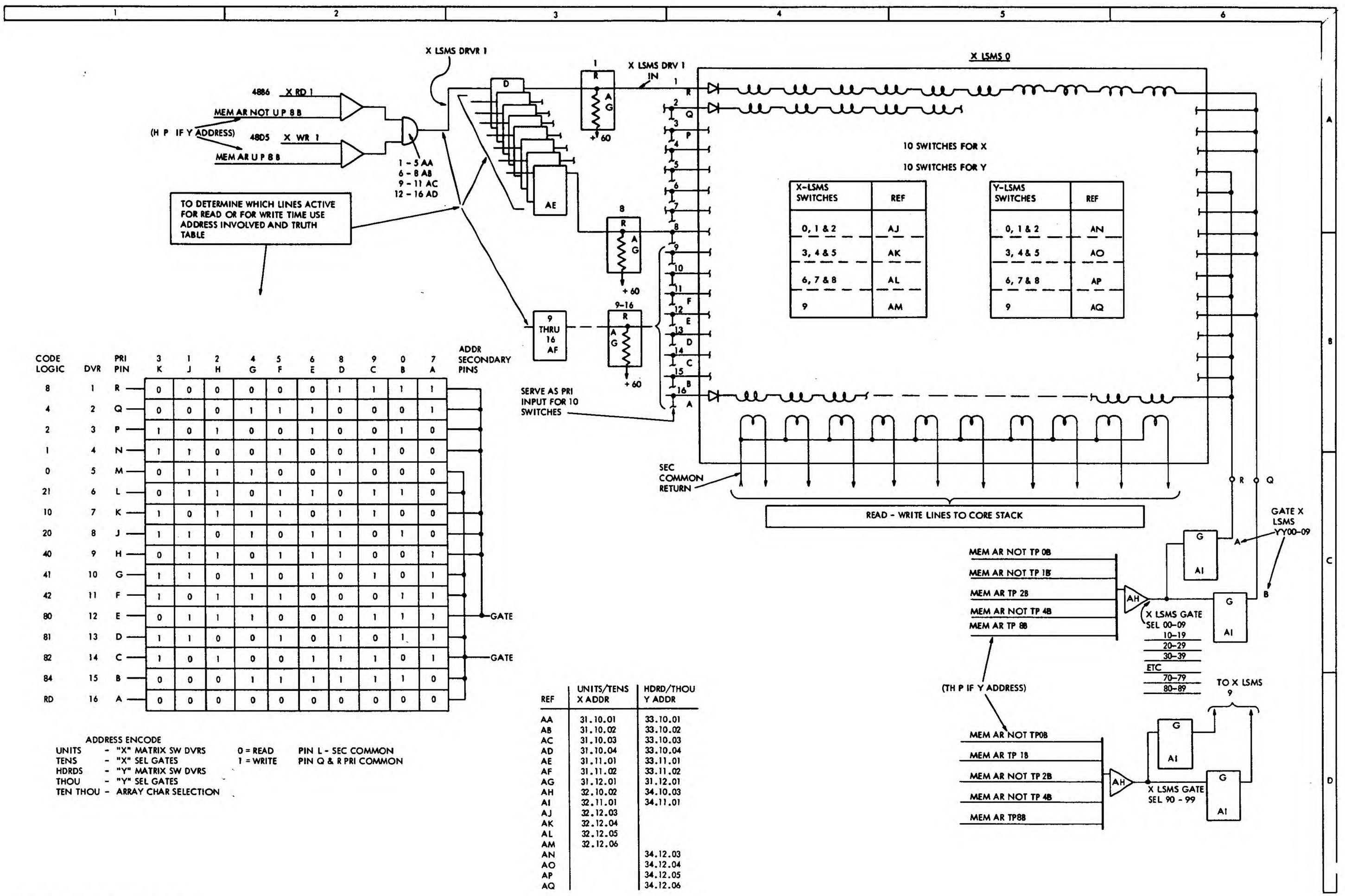


FIGURE 46. CHANNEL STATUS SAMPLE PULSES



NOTE:
FOR VOLTAGE AND CURRENT SEE FIGURE 50

FIGURE 46A. CORE STORAGE



CODE LOGIC	DVR	PRI PIN	3 K	1 J	2 H	4 G	5 F	6 E	8 D	9 C	0 B	7 A
8	1	R	0	0	0	0	0	0	1	1	1	1
4	2	Q	0	0	0	1	1	1	0	0	0	1
2	3	P	1	0	1	0	0	1	0	0	1	0
1	4	N	1	1	0	0	1	0	0	1	0	0
0	5	M	0	1	1	1	0	0	1	0	0	0
21	6	L	0	1	1	0	1	1	0	1	1	0
10	7	K	1	0	1	1	1	0	1	1	0	0
20	8	J	1	1	0	1	0	1	1	0	1	0
40	9	H	0	1	1	0	1	1	1	0	0	1
41	10	G	1	1	0	1	0	1	0	1	0	1
42	11	F	1	0	1	1	1	0	0	0	1	1
80	12	E	0	1	1	1	0	0	0	1	1	1
81	13	D	1	1	0	0	1	0	1	0	1	1
82	14	C	1	0	1	0	0	1	1	1	0	1
84	15	B	0	0	0	1	1	1	1	1	1	0
RD	16	A	0	0	0	0	0	0	0	0	0	0

ADDR SECONDARY PINS

GATE

GATE

ADDRESS ENCODE
UNITS - "X" MATRIX SW DVRS
TENS - "X" SEL GATES
HDRDS - "Y" MATRIX SW DVRS
THOU - "Y" SEL GATES
TEN THOU - ARRAY CHAR SELECTION

0 = READ
1 = WRITE

PIN L - SEC COMMON
PIN Q & R PRI COMMON

REF	UNITS/TENS X ADDR	HDRD/THOU Y ADDR
AA	31.10.01	33.10.01
AB	31.10.02	33.10.02
AC	31.10.03	33.10.03
AD	31.10.04	33.10.04
AE	31.11.01	33.11.01
AF	31.11.02	33.11.02
AG	31.12.01	31.12.01
AH	32.10.02	34.10.03
AI	32.11.01	34.11.01
AJ	32.12.03	
AK	32.12.04	
AL	32.12.05	
AM	32.12.06	
AN		34.12.03
AO		34.12.04
AP		34.12.05
AQ		34.12.06

FIGURE 47. LSMS, PRI DRVRS, & GATE SEL

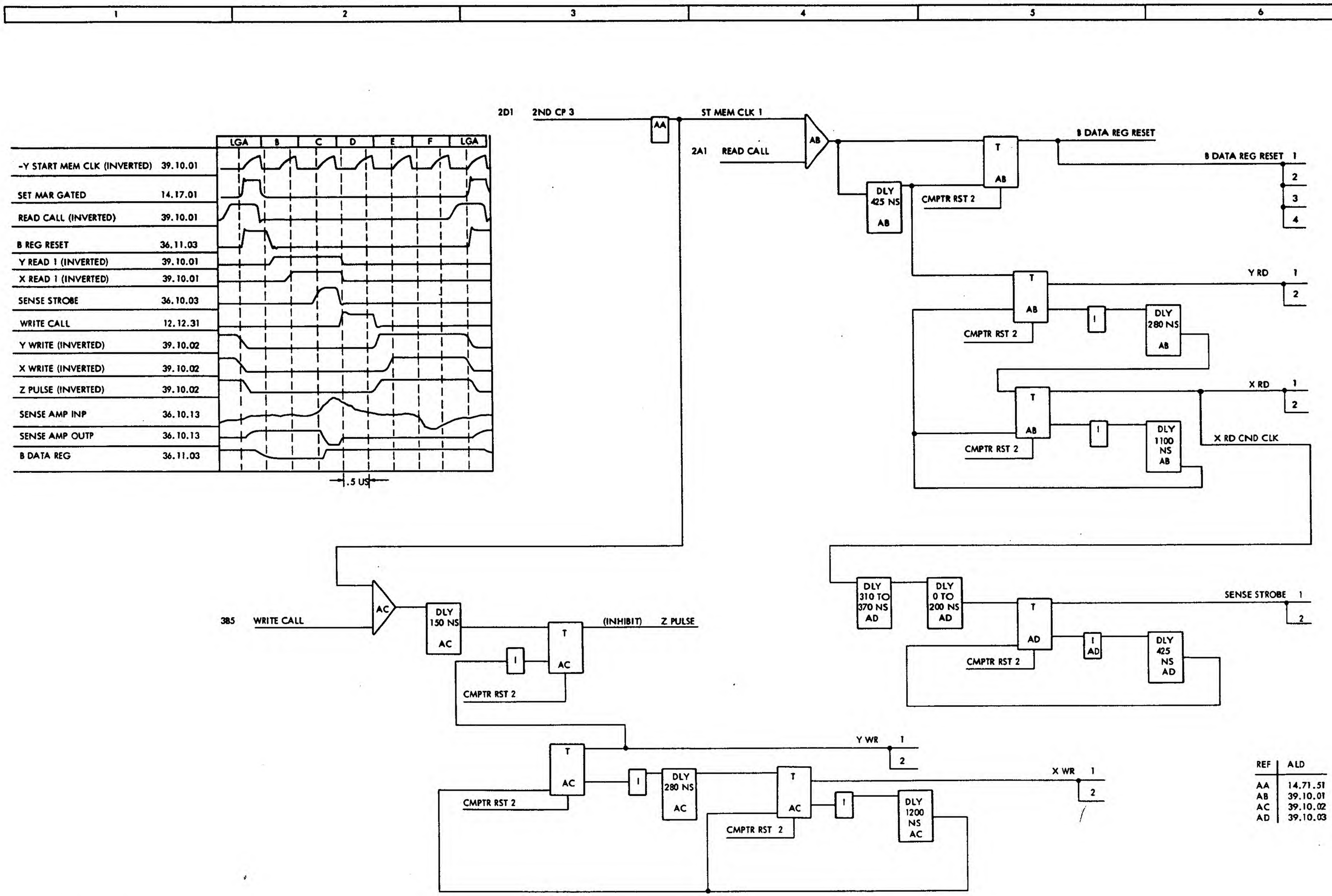
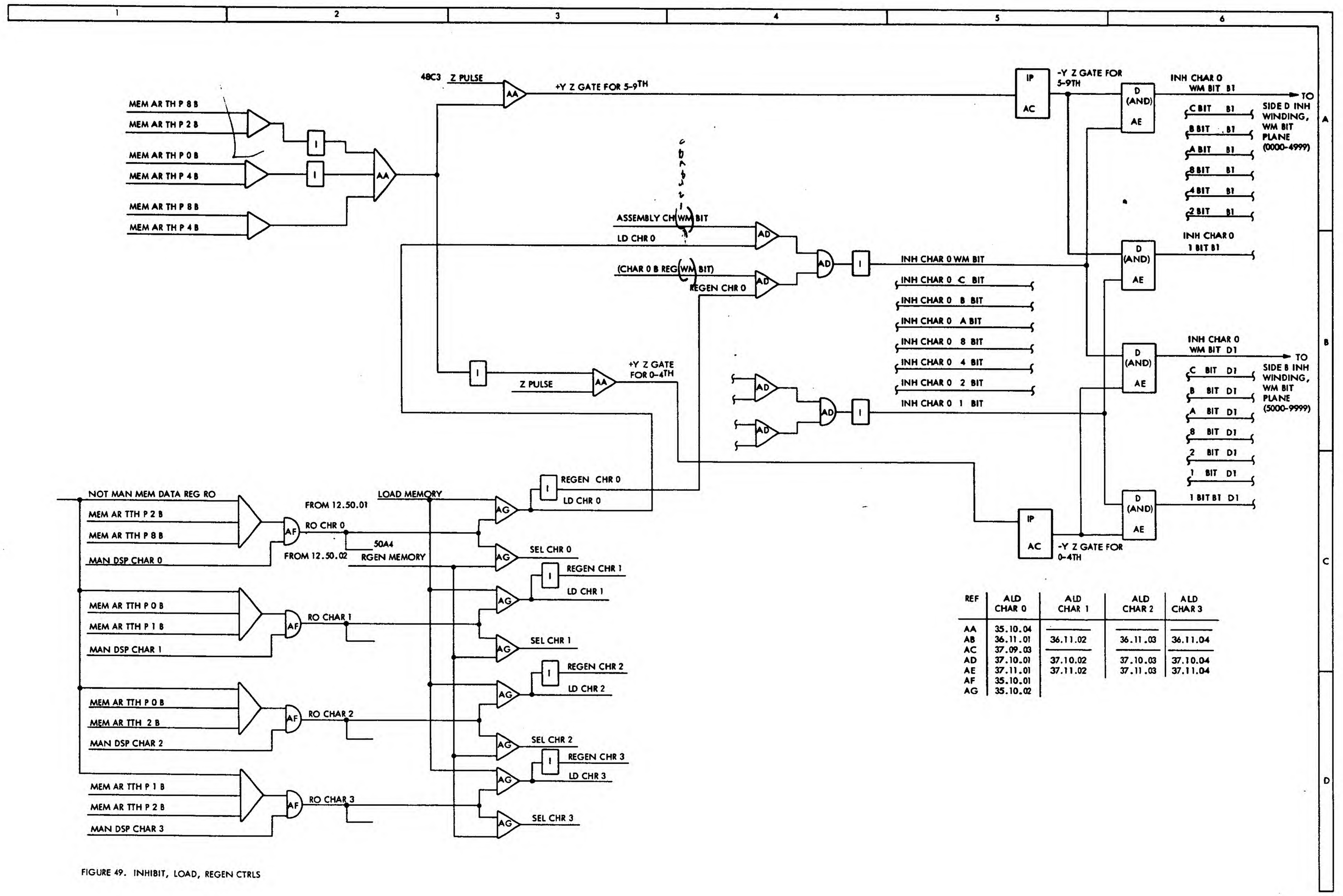
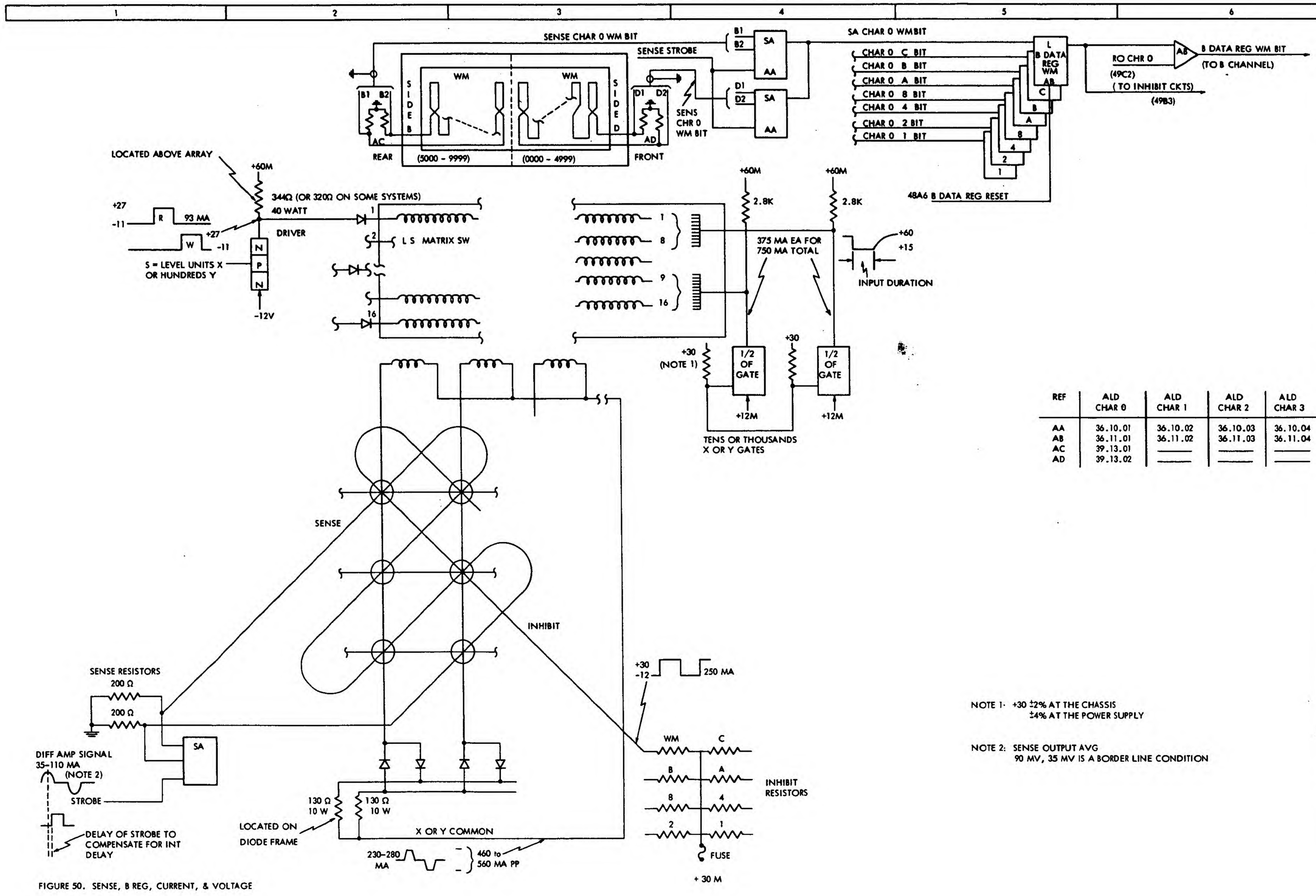


FIGURE 48. MEM CLOCK TIMING



REF	ALD CHAR 0	ALD CHAR 1	ALD CHAR 2	ALD CHAR 3
AA	35.10.04	—	—	—
AB	36.11.01	36.11.02	36.11.03	36.11.04
AC	37.09.03	—	—	—
AD	37.10.01	37.10.02	37.10.03	37.10.04
AE	37.11.01	37.11.02	37.11.03	37.11.04
AF	35.10.01			
AG	35.10.02			

FIGURE 49. INHIBIT, LOAD, REGEN CTRLS



REF	ALD CHAR 0	ALD CHAR 1	ALD CHAR 2	ALD CHAR 3
AA	36.10.01	36.10.02	36.10.03	36.10.04
AB	36.11.01	36.11.02	36.11.03	36.11.04
AC	39.13.01	———	———	———
AD	39.13.02	———	———	———

NOTE 1: +30 ±2% AT THE CHASSIS
±4% AT THE POWER SUPPLY

NOTE 2: SENSE OUTPUT AVG
90 MV, 35 MV IS A BORDER LINE CONDITION

FIGURE 50. SENSE, B REG, CURRENT, & VOLTAGE

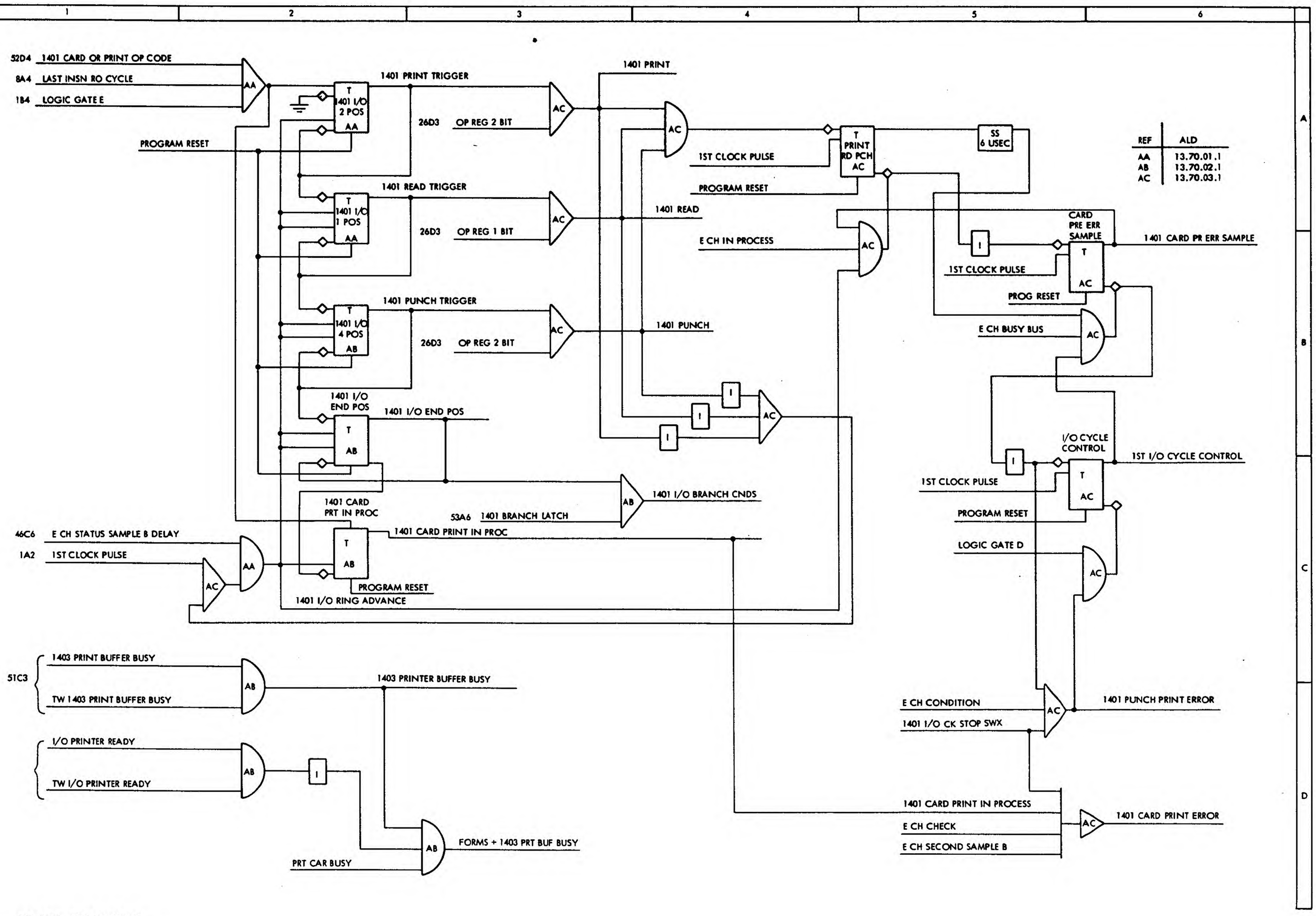
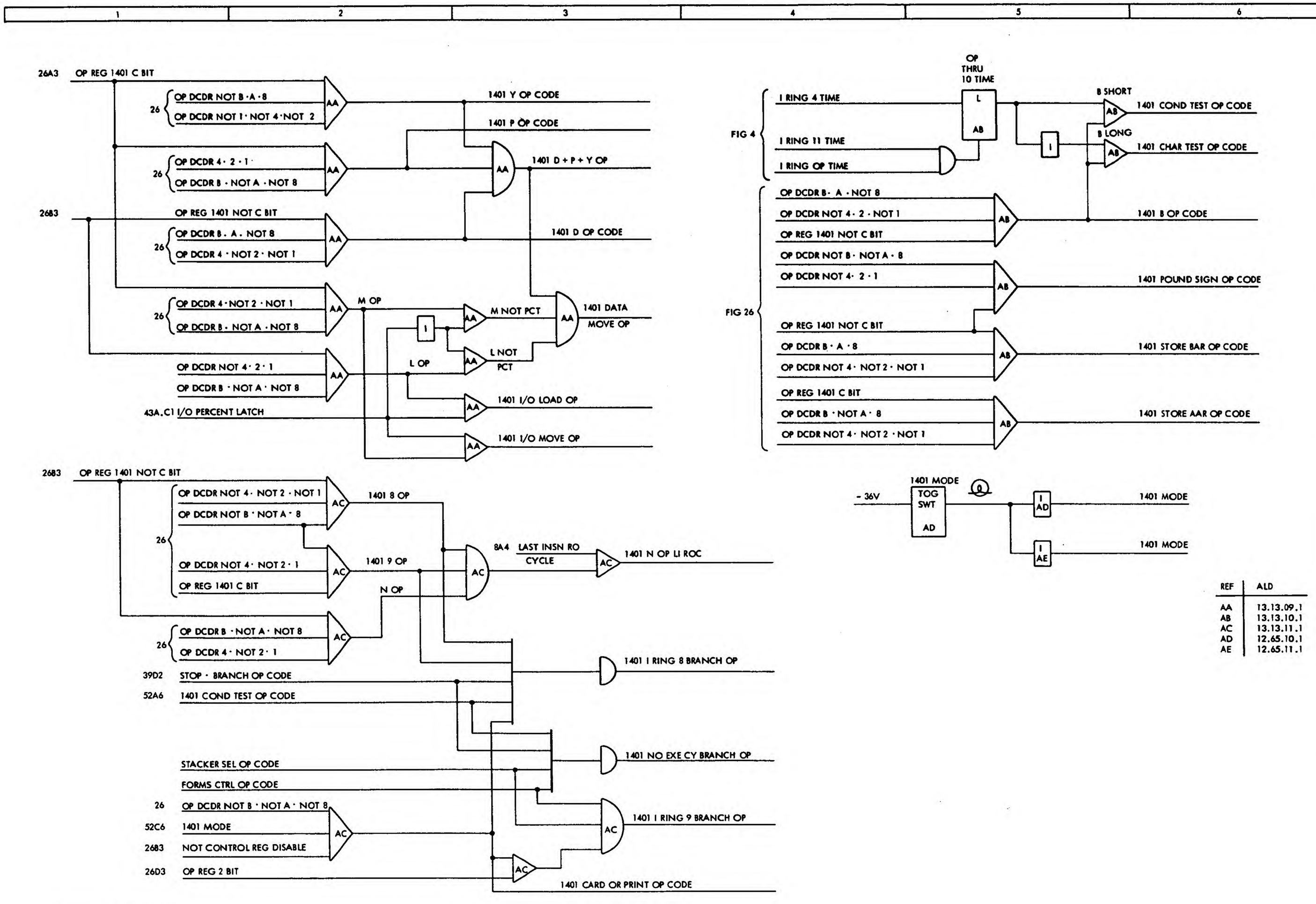
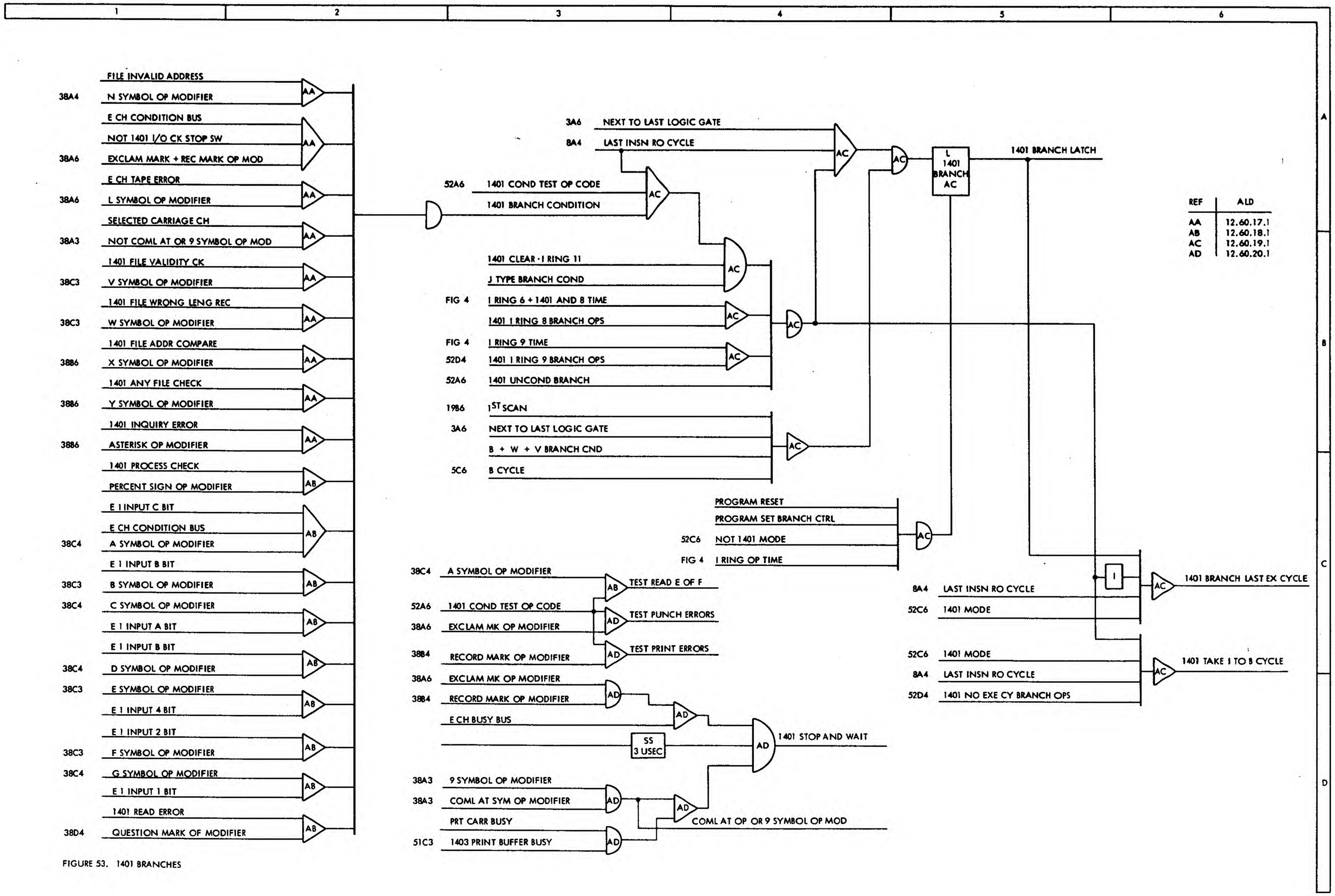


FIGURE 51. 1401 BUFFER CTRL



REF	ALD
AA	13.13.09.1
AB	13.13.10.1
AC	13.13.11.1
AD	12.65.10.1
AE	12.65.11.1

FIGURE 52. 1401 OP DECODE



REF	ALD
AA	12.60.17.1
AB	12.60.18.1
AC	12.60.19.1
AD	12.60.20.1

FIGURE 53. 1401 BRANCHES

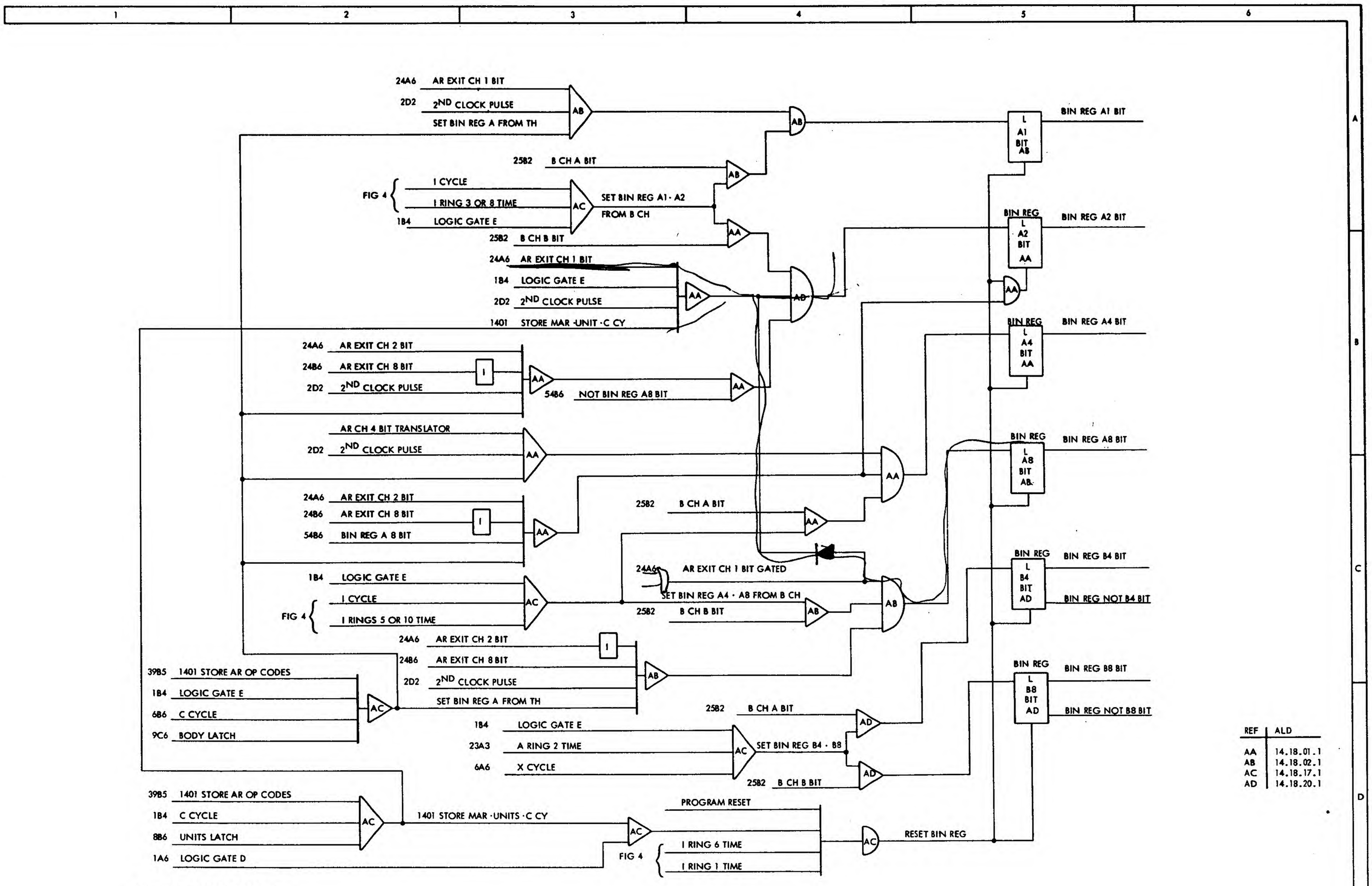


FIGURE 54. BIN REG & SET CTRL

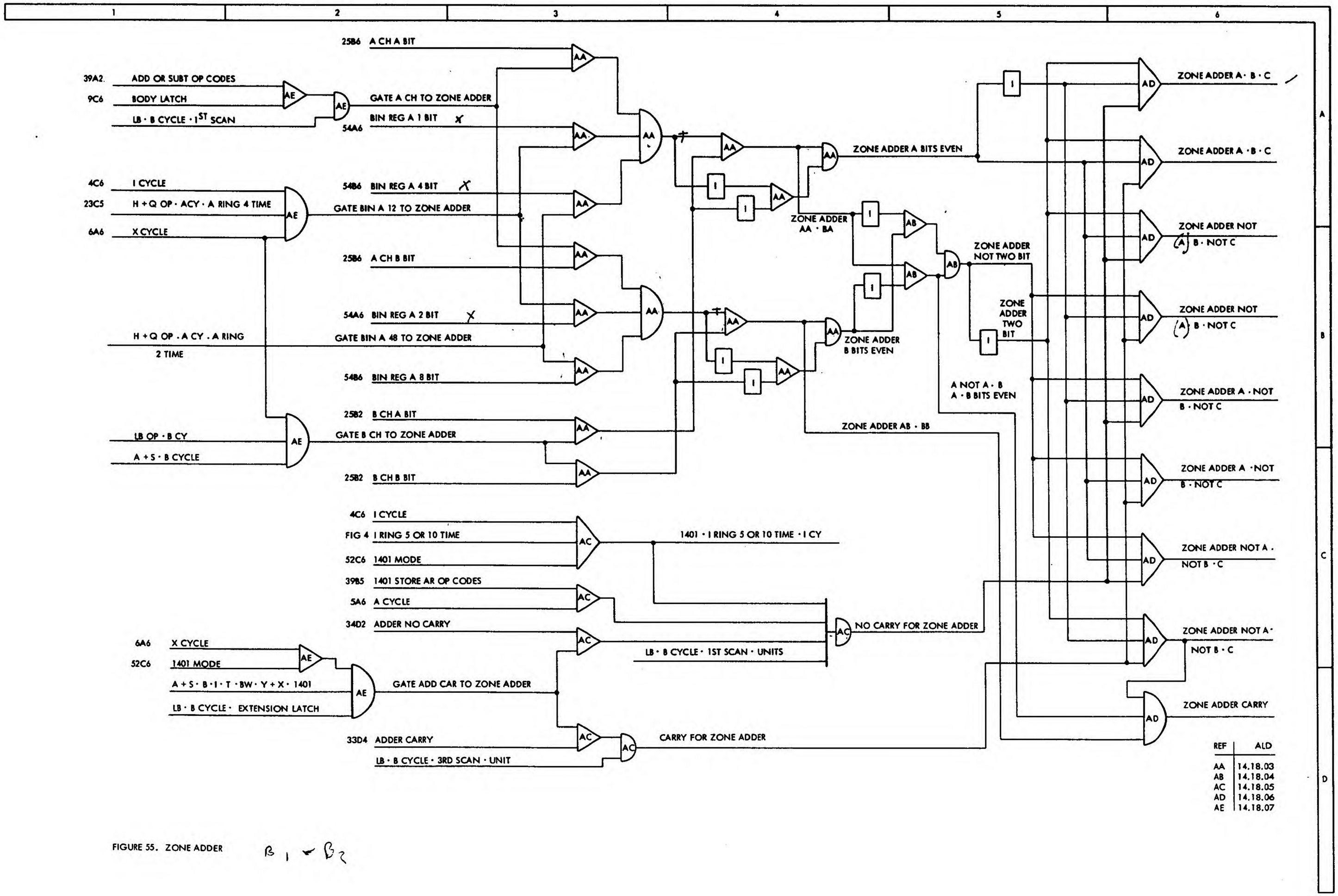


FIGURE 55. ZONE ADDER

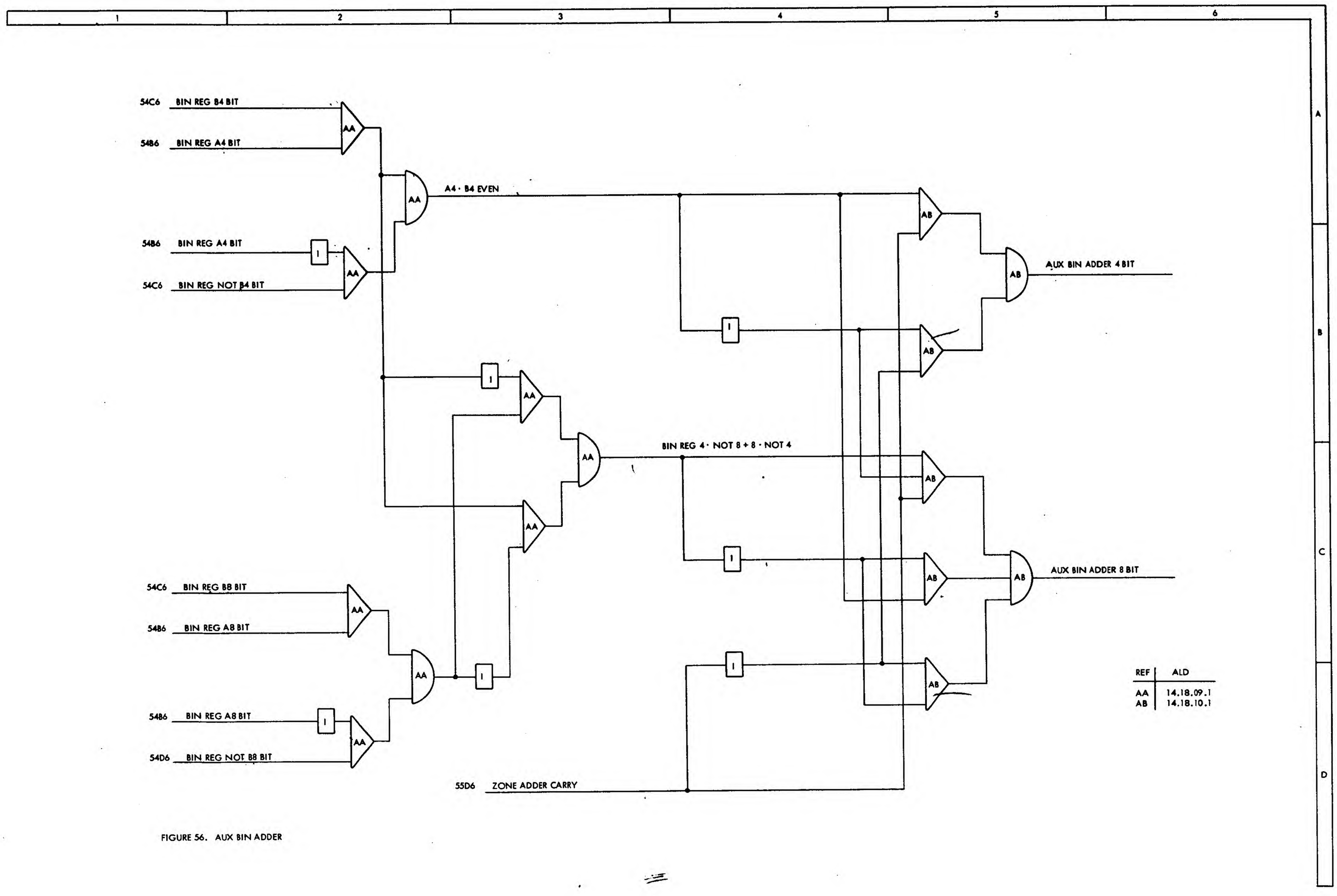
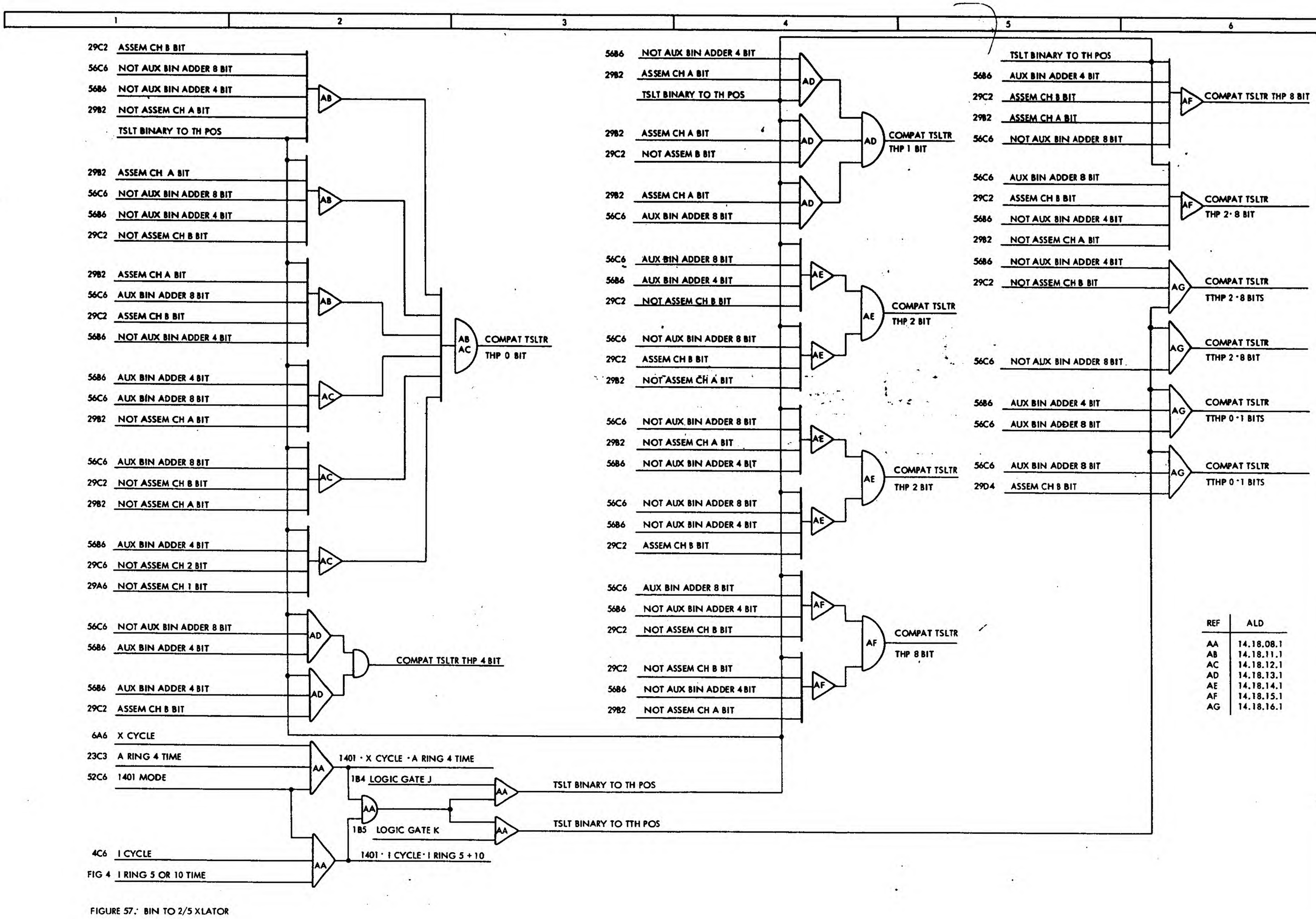


FIGURE 56. AUX BIN ADDER



REF	ALD
AA	14.18.08.1
AB	14.18.11.1
AC	14.18.12.1
AD	14.18.13.1
AE	14.18.14.1
AF	14.18.15.1
AG	14.18.16.1

FIGURE 57. BIN TO 2/5 XLATOR

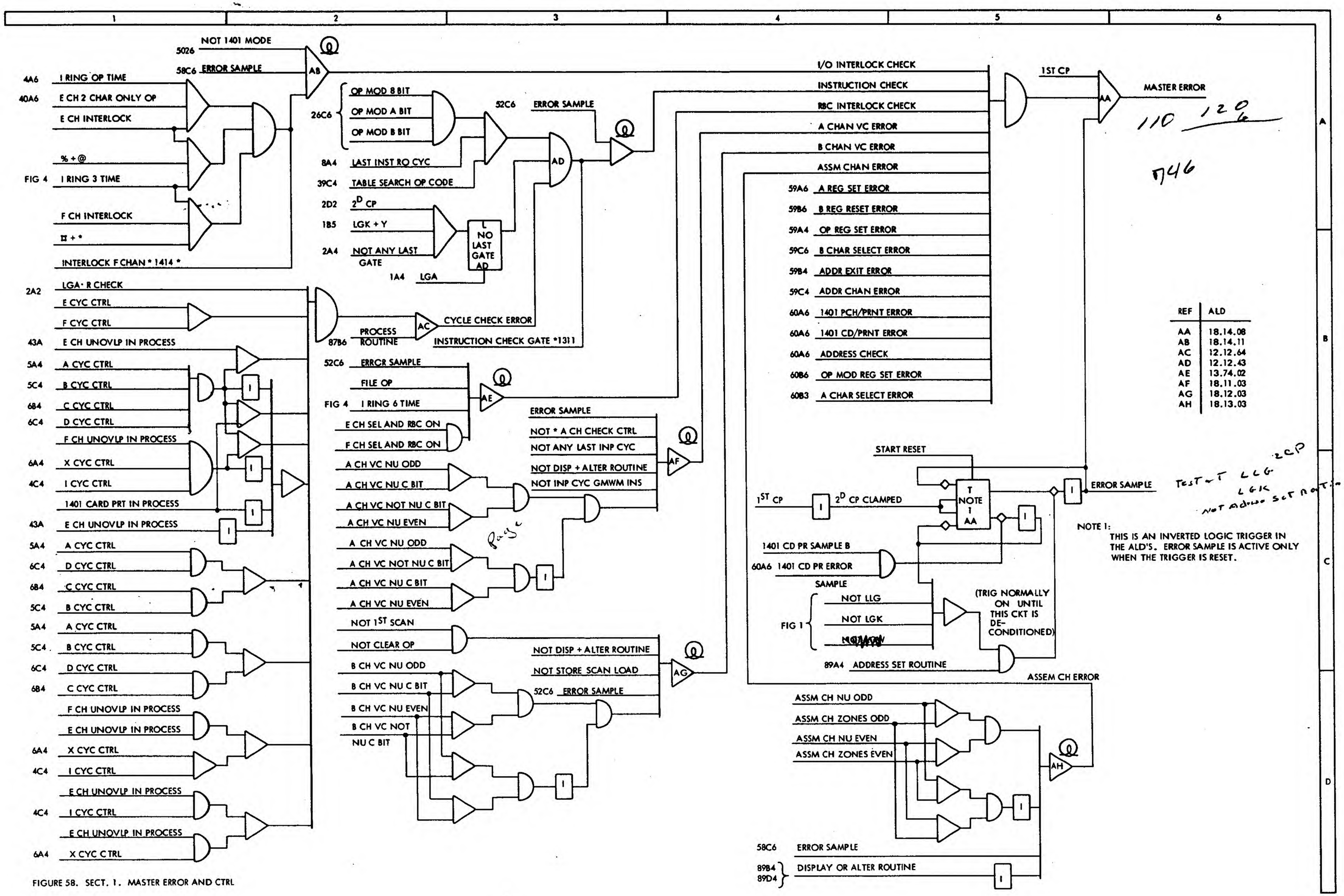
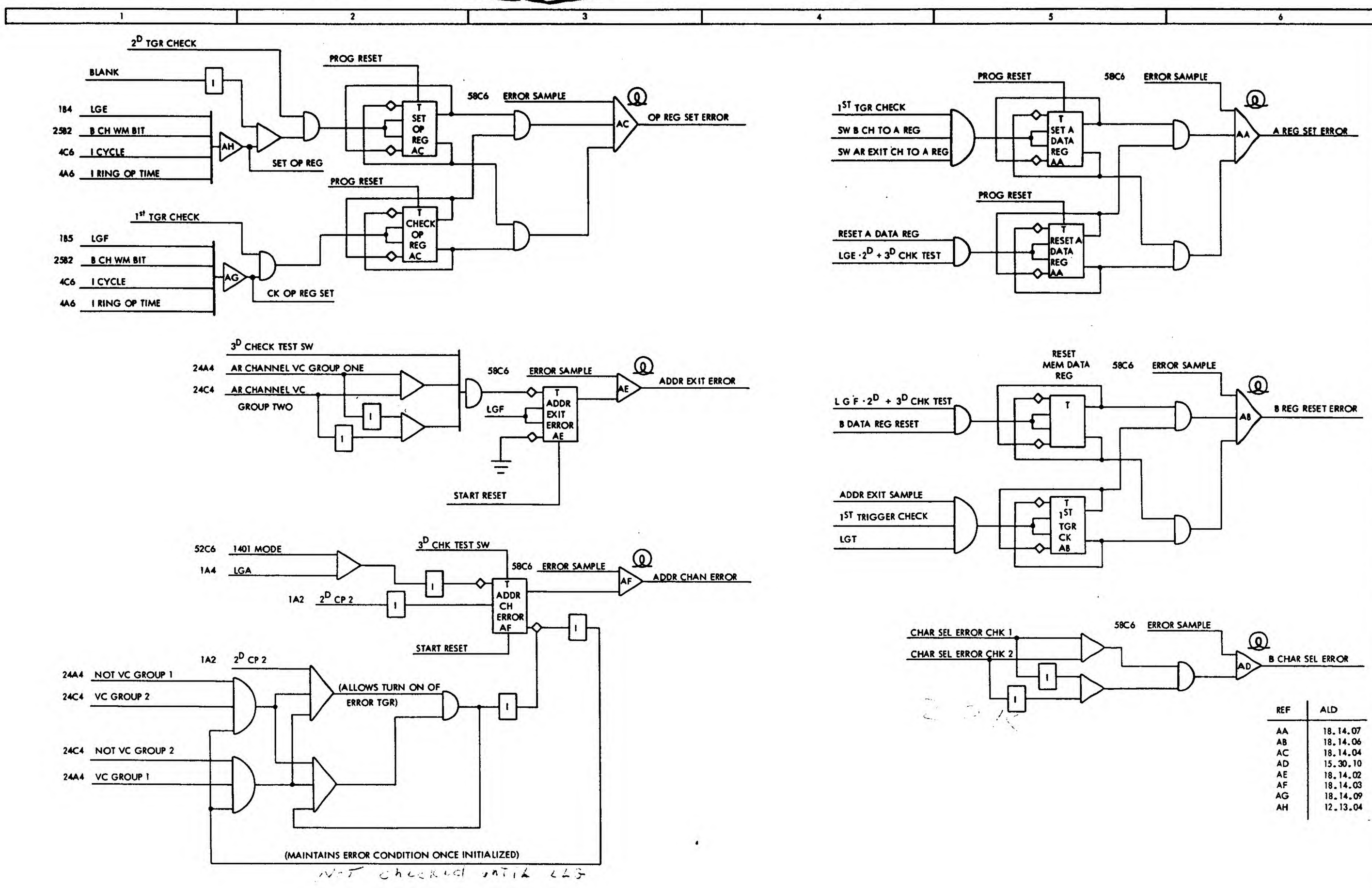


FIGURE 58. SECT. 1. MASTER ERROR AND CTRL



REF	ALD
AA	18.14.07
AB	18.14.06
AC	18.14.04
AD	15.30.10
AE	18.14.02
AF	18.14.03
AG	18.14.09
AH	12.13.04

FIGURE 59. SECT 2 MASTER ERROR & CTRL

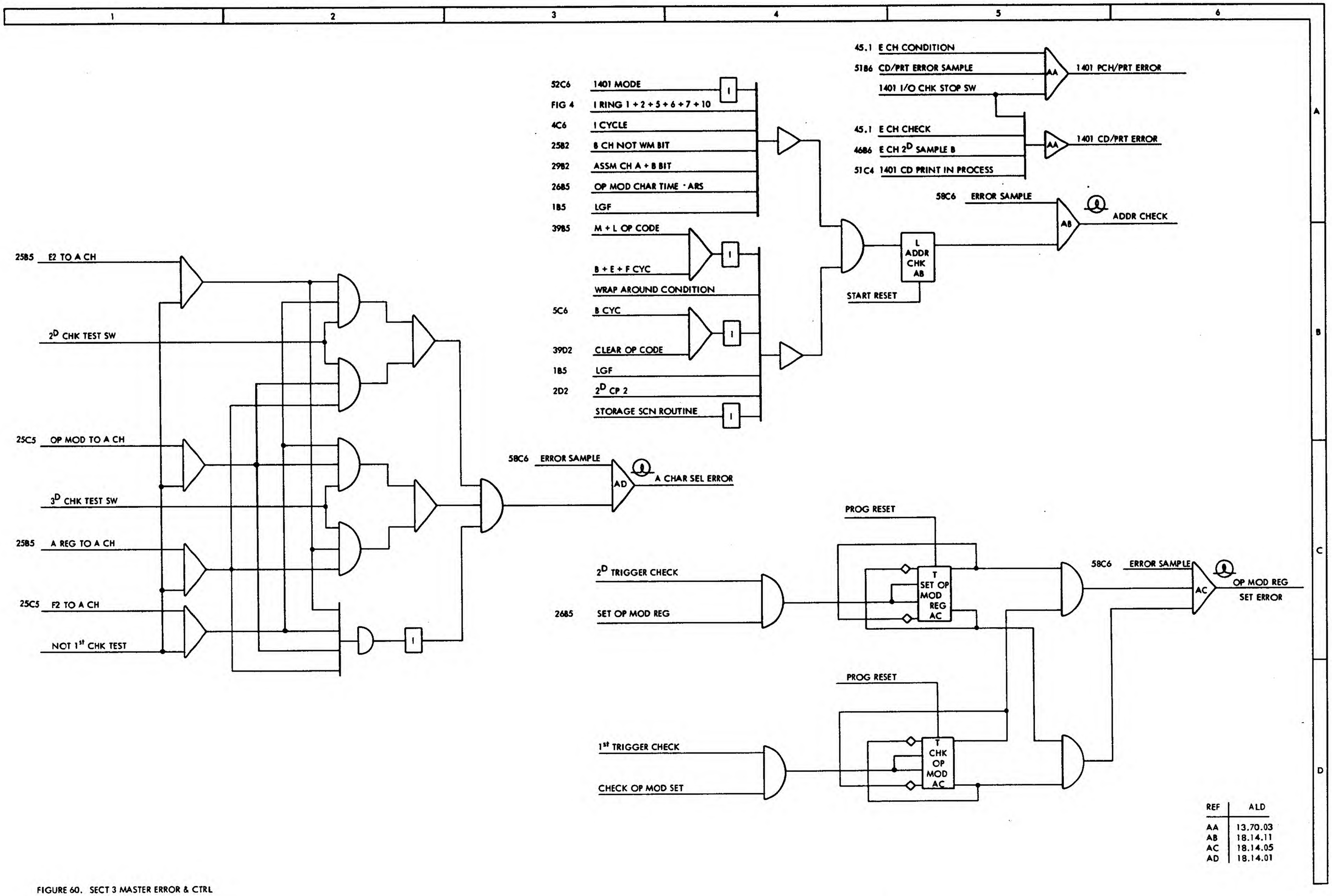


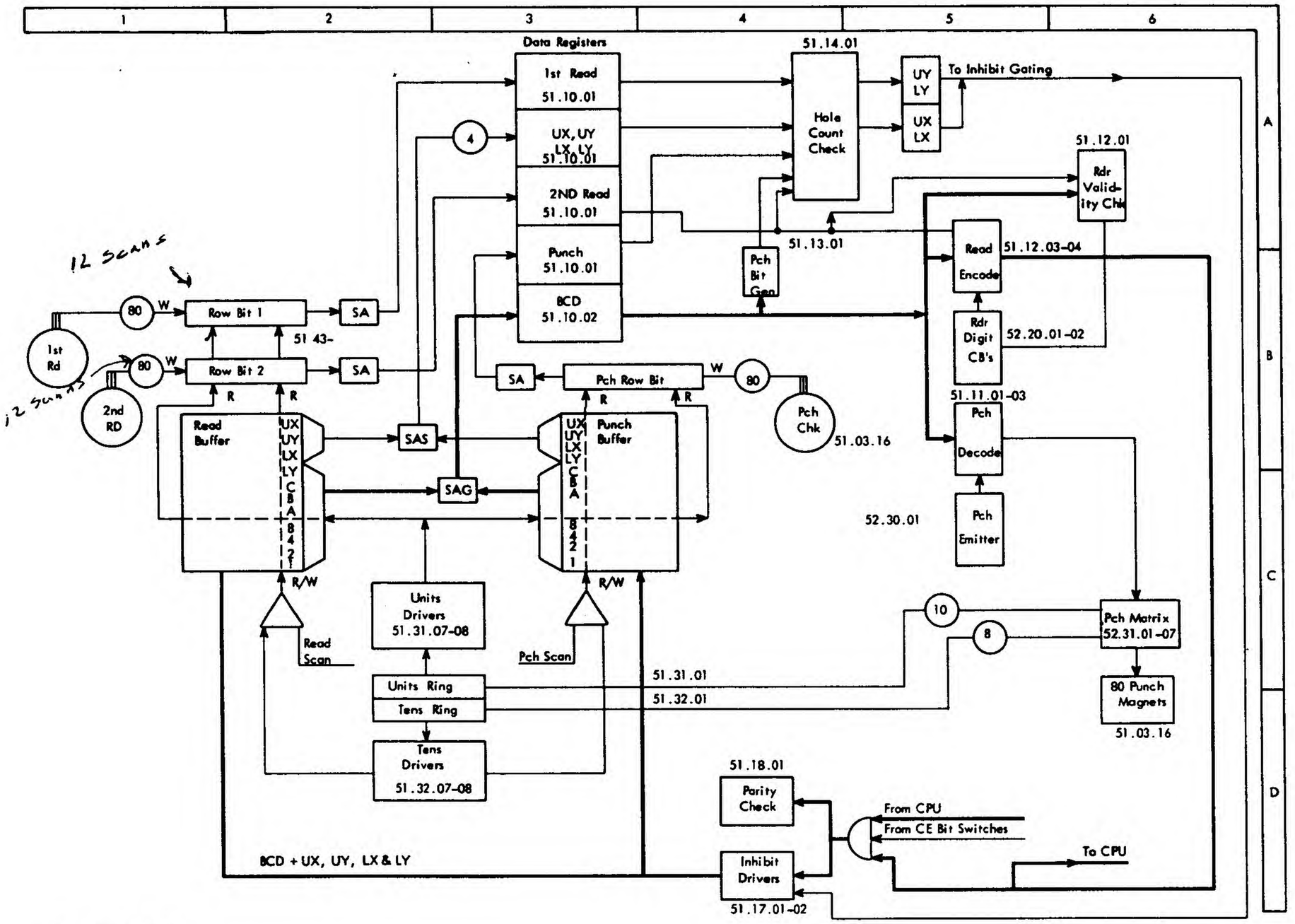
FIGURE 60. SECT 3 MASTER ERROR & CTRL

Run in 12 1st Read 12 2nd read

M 9011 1 cpu 12 scans To Buffer

M 9019 1 cpu (Two Feed cycle)

Kd 12 Scans To Buffer



(Heavy Line is BCD)

FIGURE 61A. INT BFR DATA FLOW

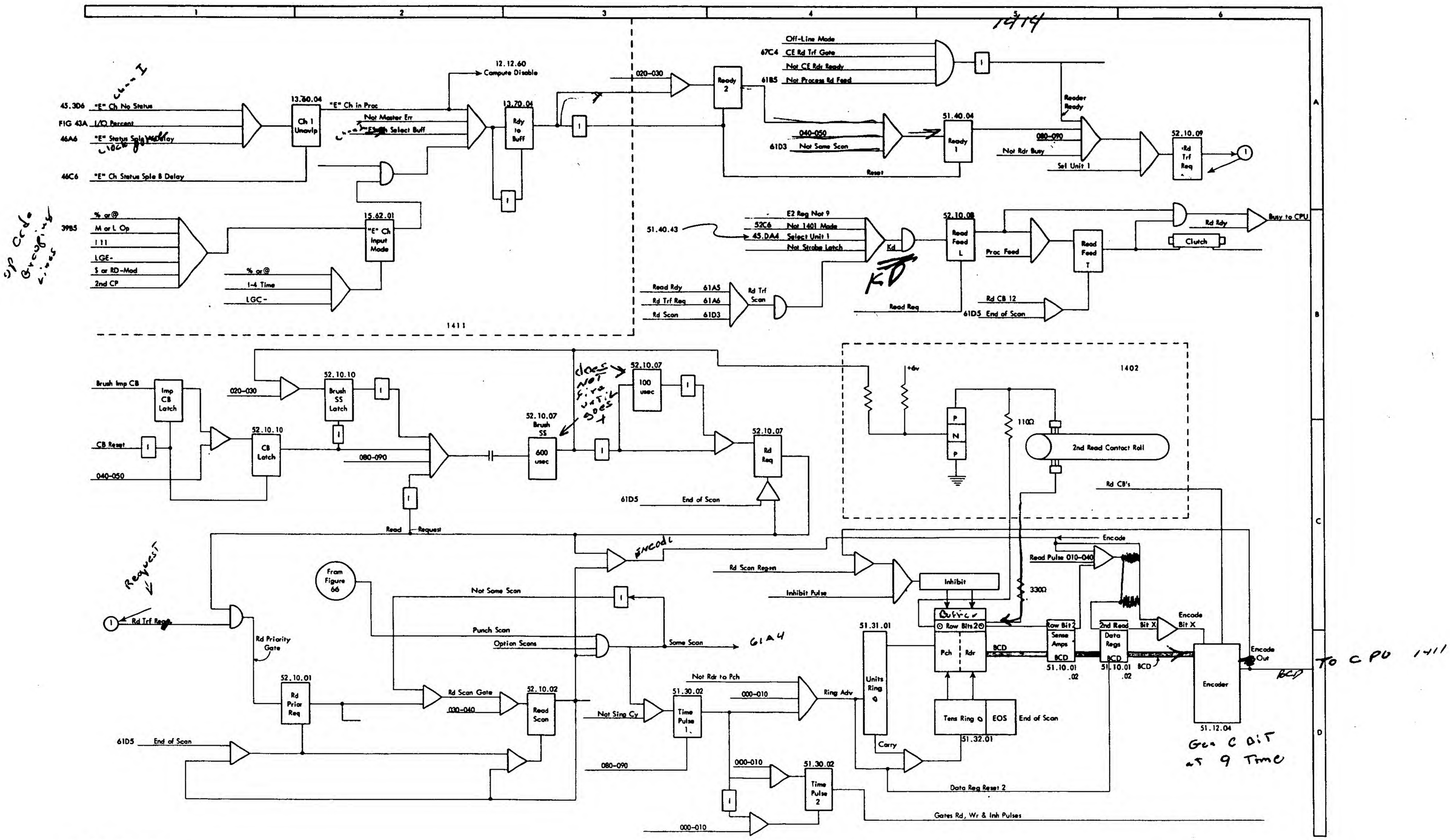
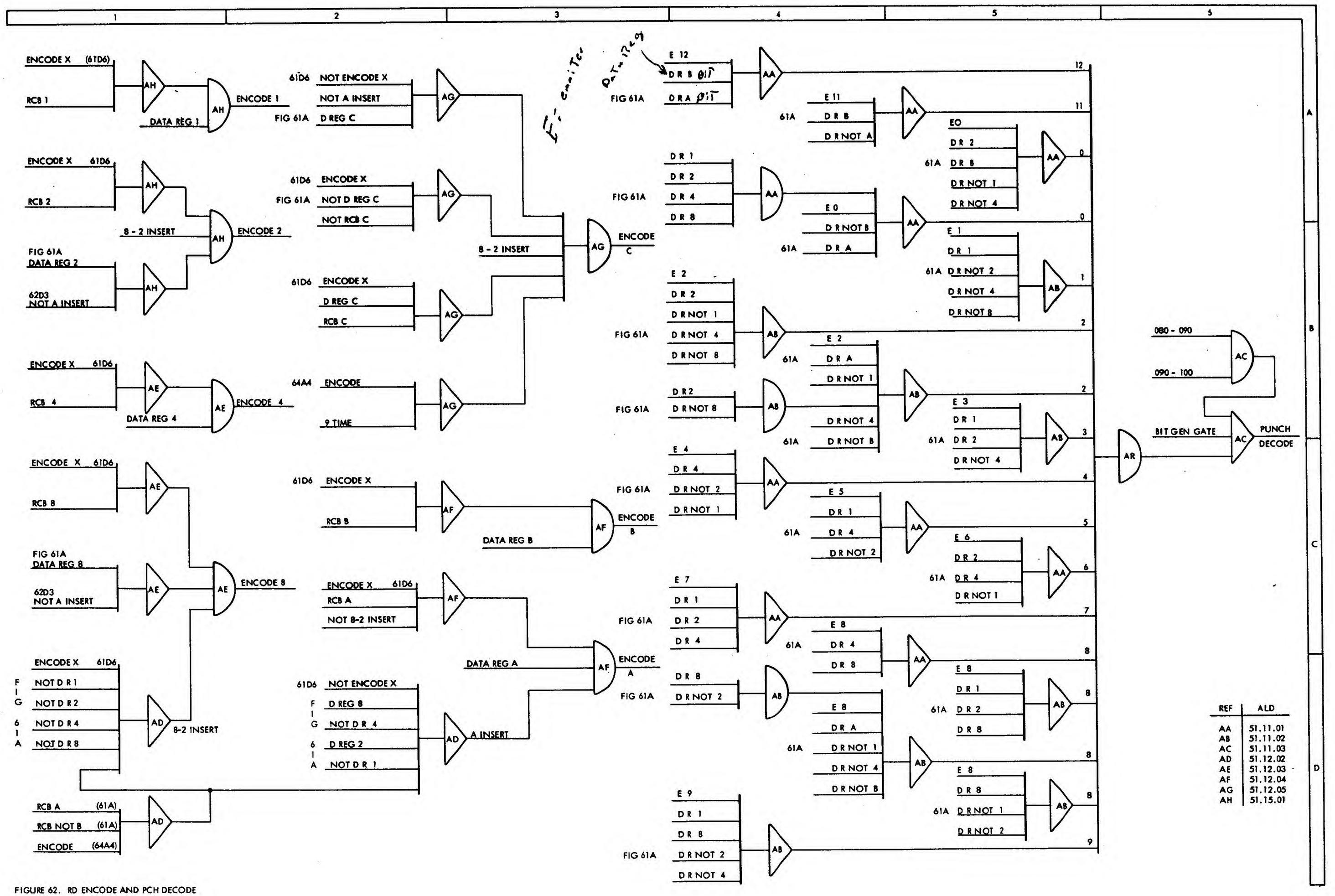


FIGURE 61. READER CONTROL



REF	ALD
AA	51.11.01
AB	51.11.02
AC	51.11.03
AD	51.12.02
AE	51.12.03
AF	51.12.04
AG	51.12.05
AH	51.15.01

FIGURE 62. RD ENCODE AND PCH DECODE

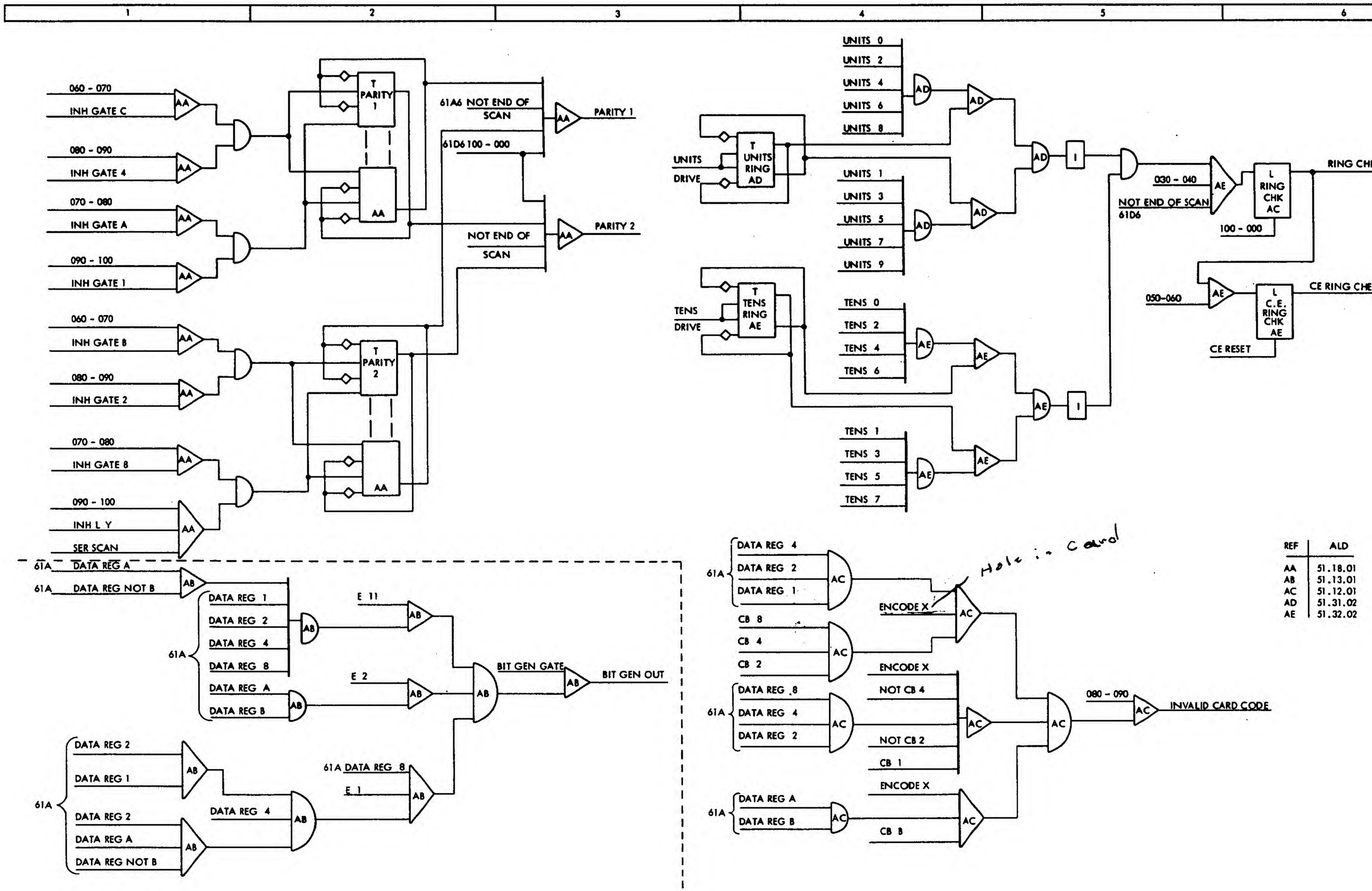


FIGURE 63. INT BUFFER CHECKS AND PUNCH BIT GENERATE

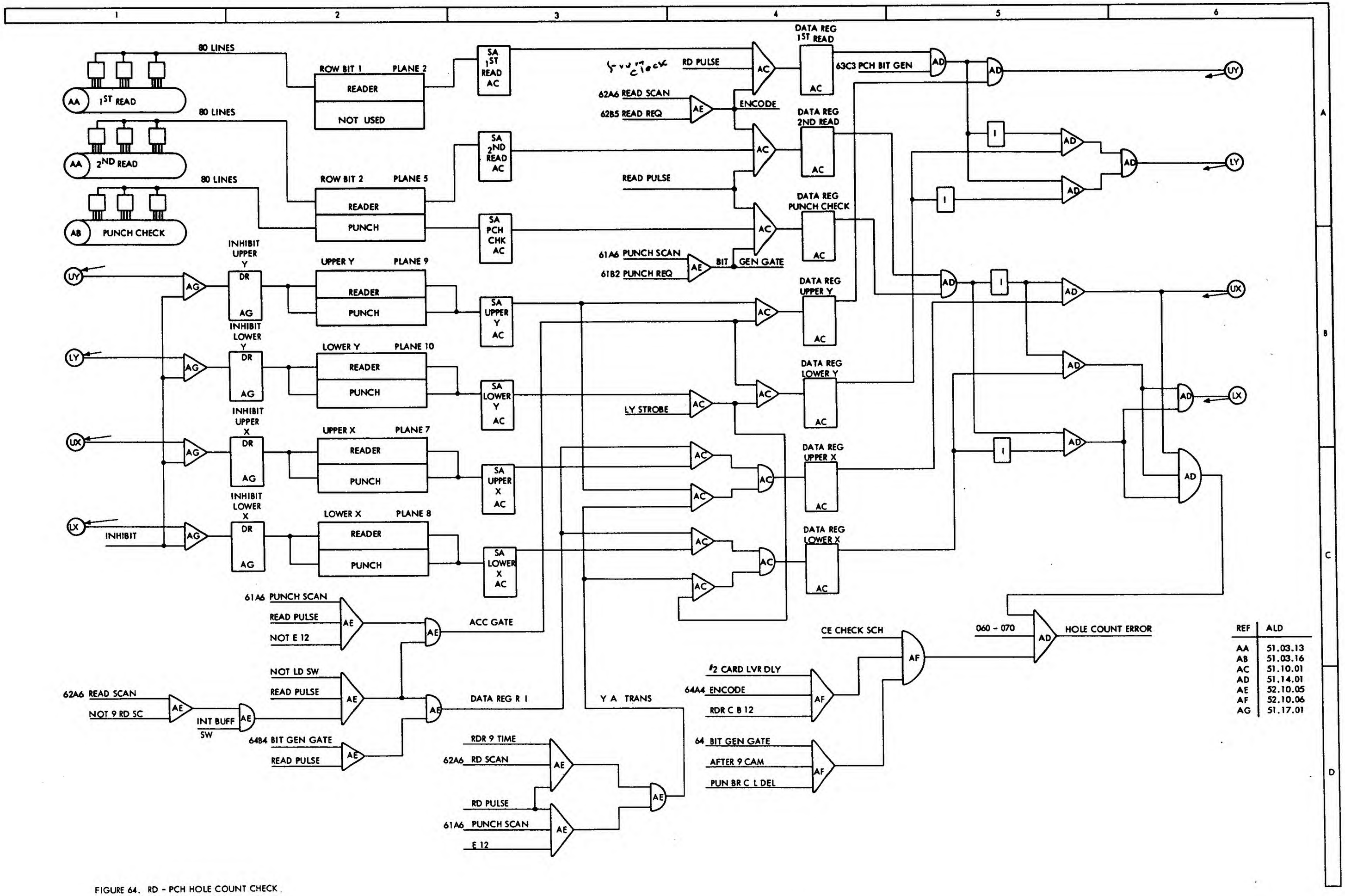


FIGURE 64. RD - PCH HOLE COUNT CHECK.

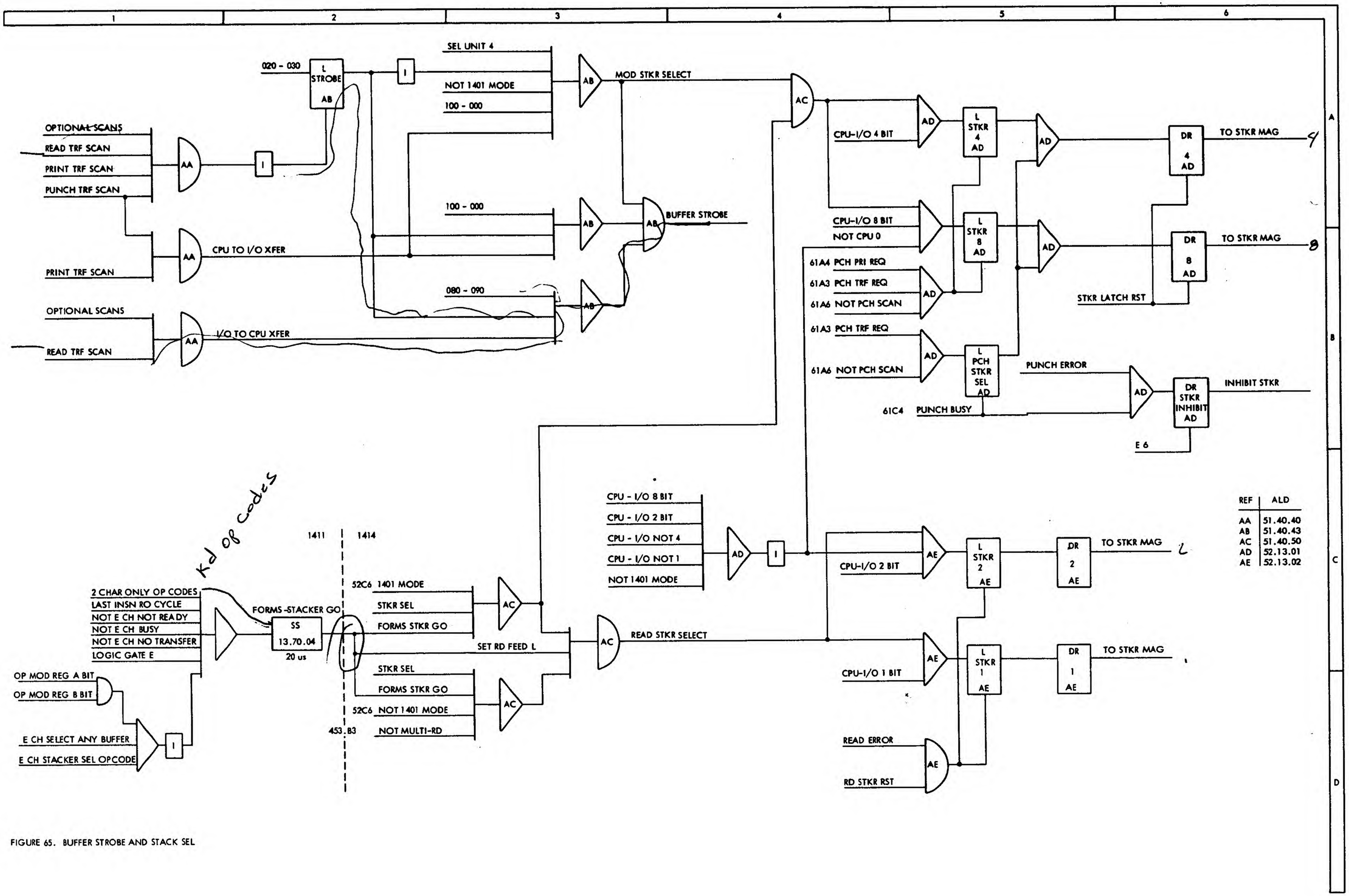


FIGURE 65. BUFFER STROBE AND STACK SEL

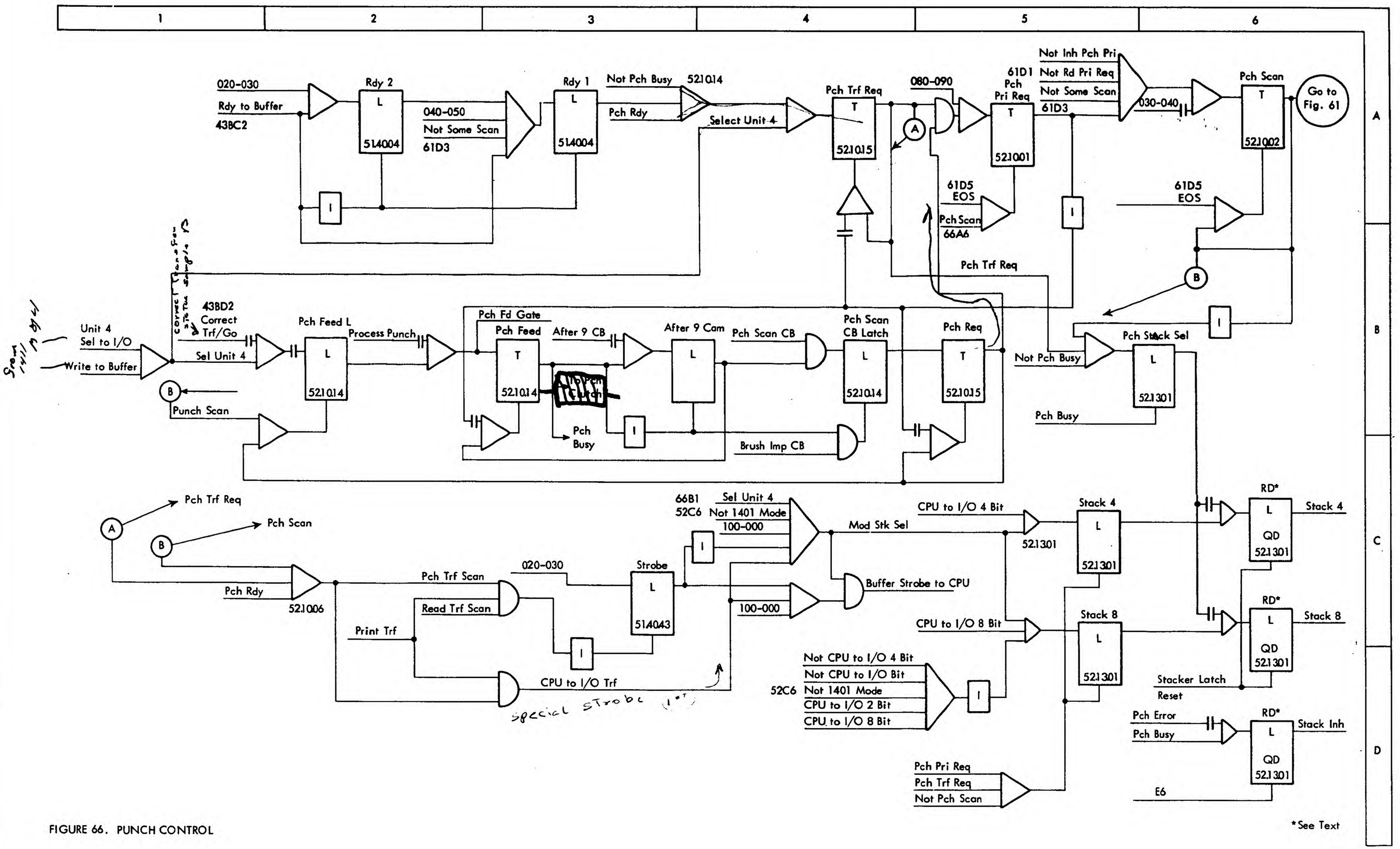


FIGURE 66. PUNCH CONTROL

*See Text

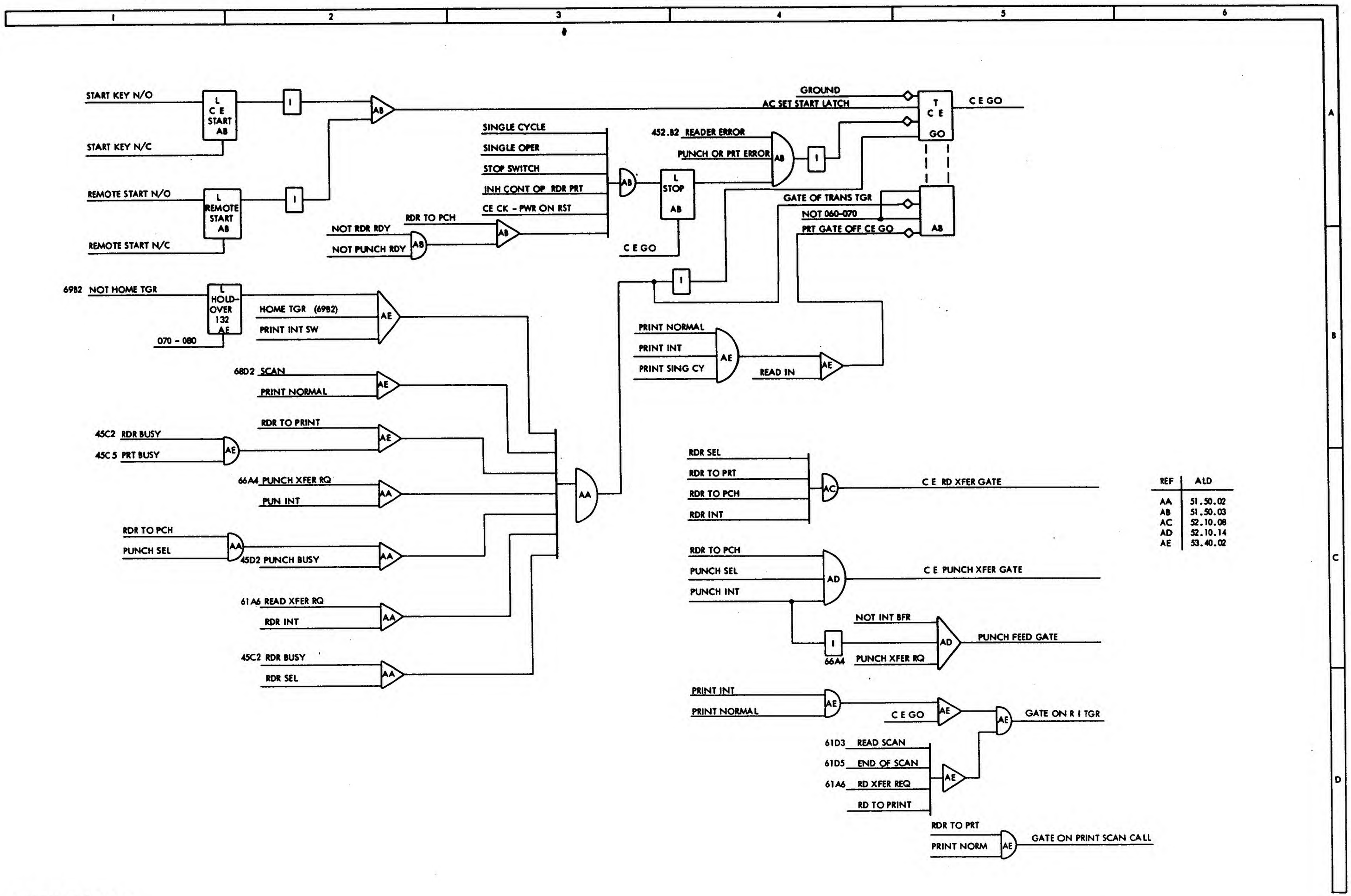


FIGURE 67. 1414-3 C E GO

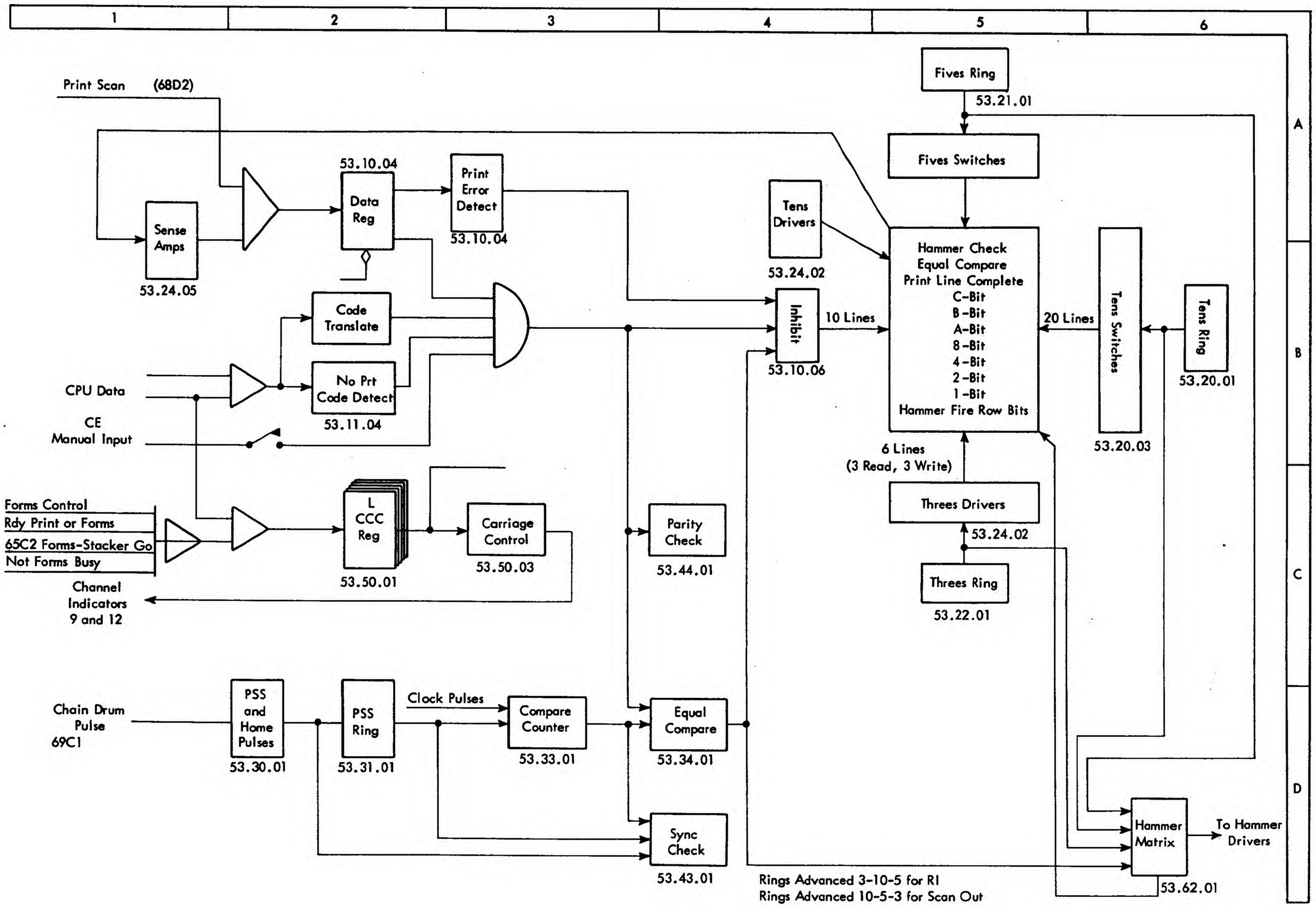


FIGURE 68A. PRINT STORAGE DATA FLOW

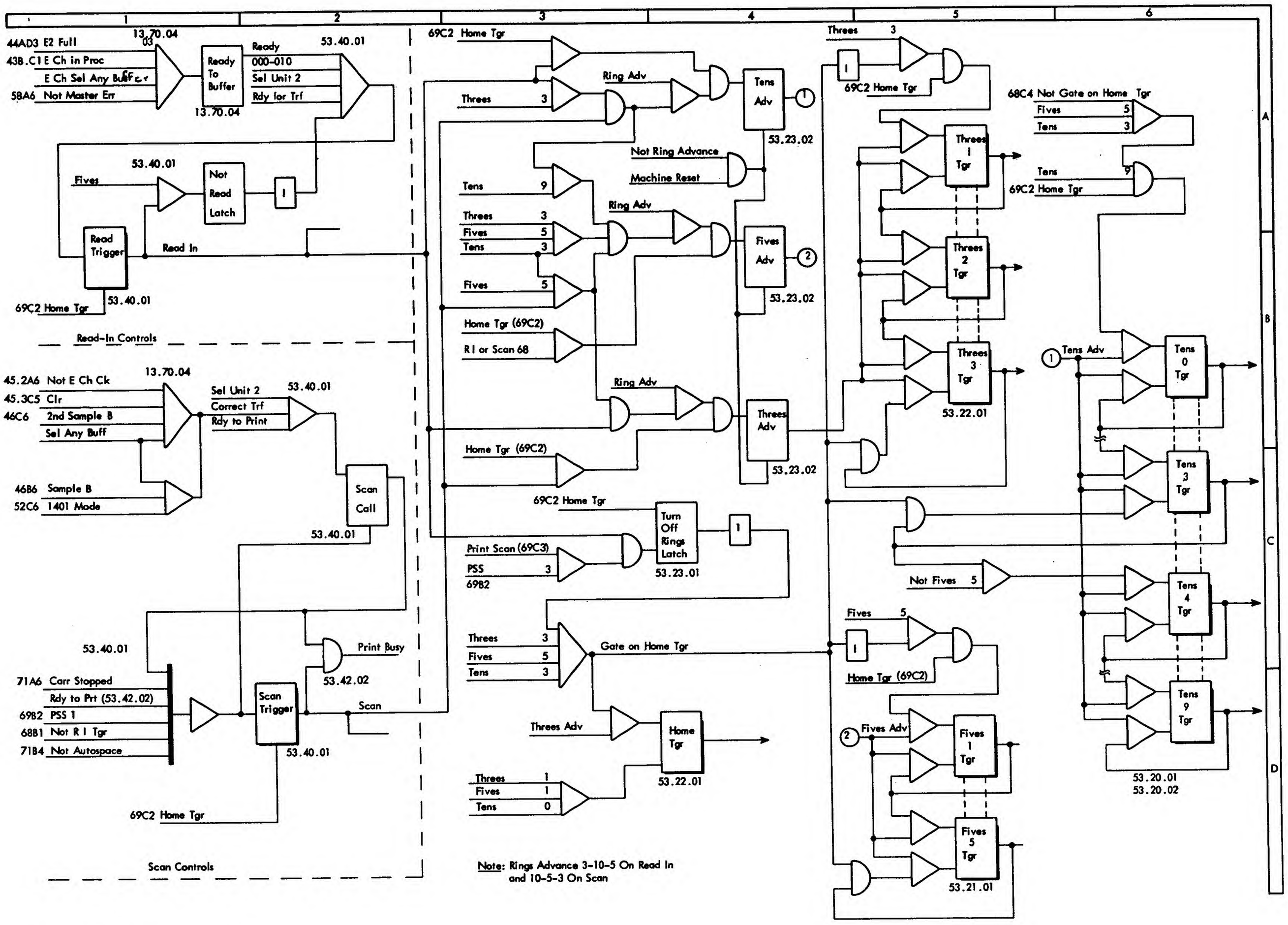


FIGURE 68. PRINT CTRL AND PRINT BFR RINGS

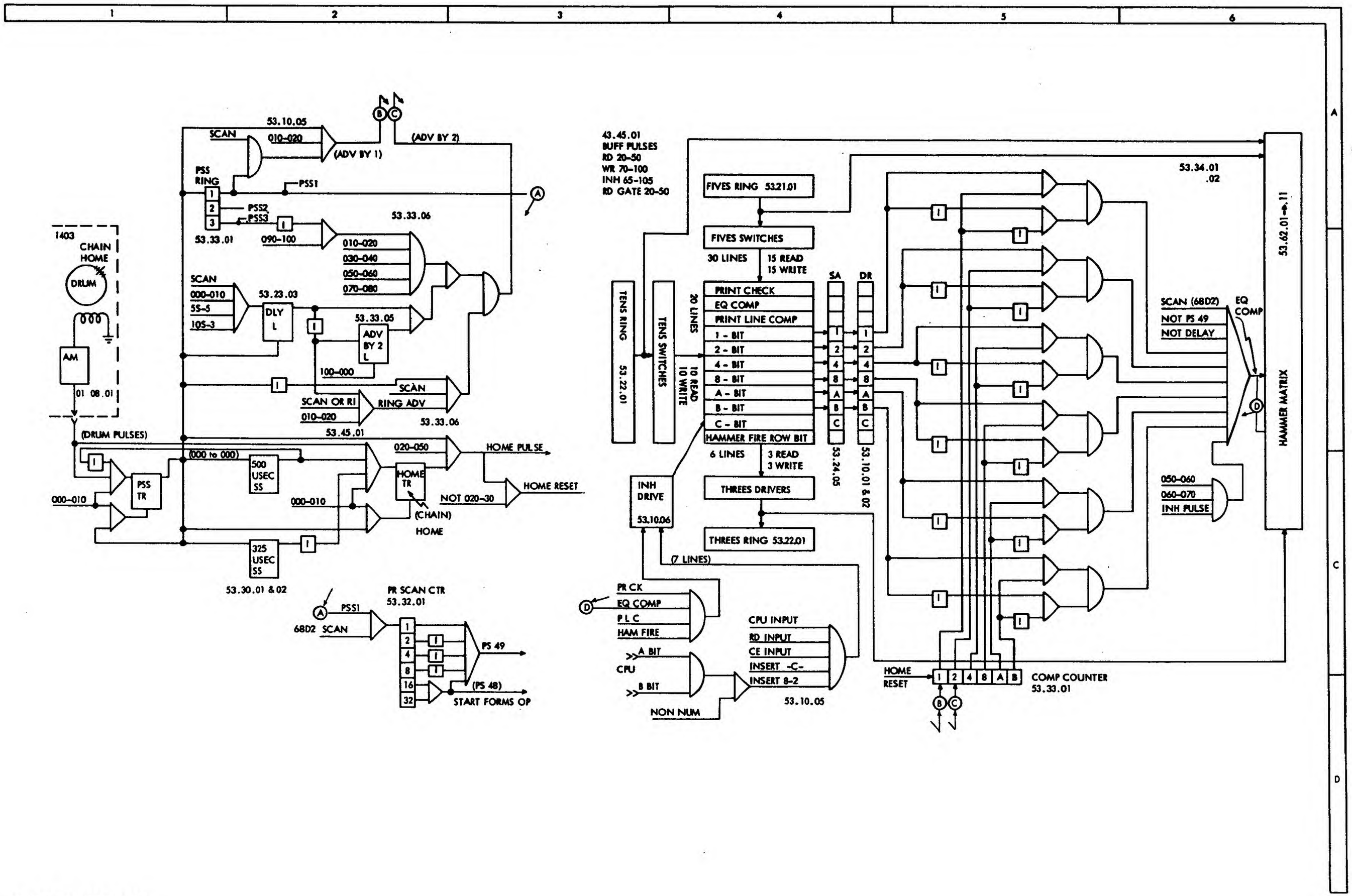


FIGURE 69. - PRINT CONTROLS

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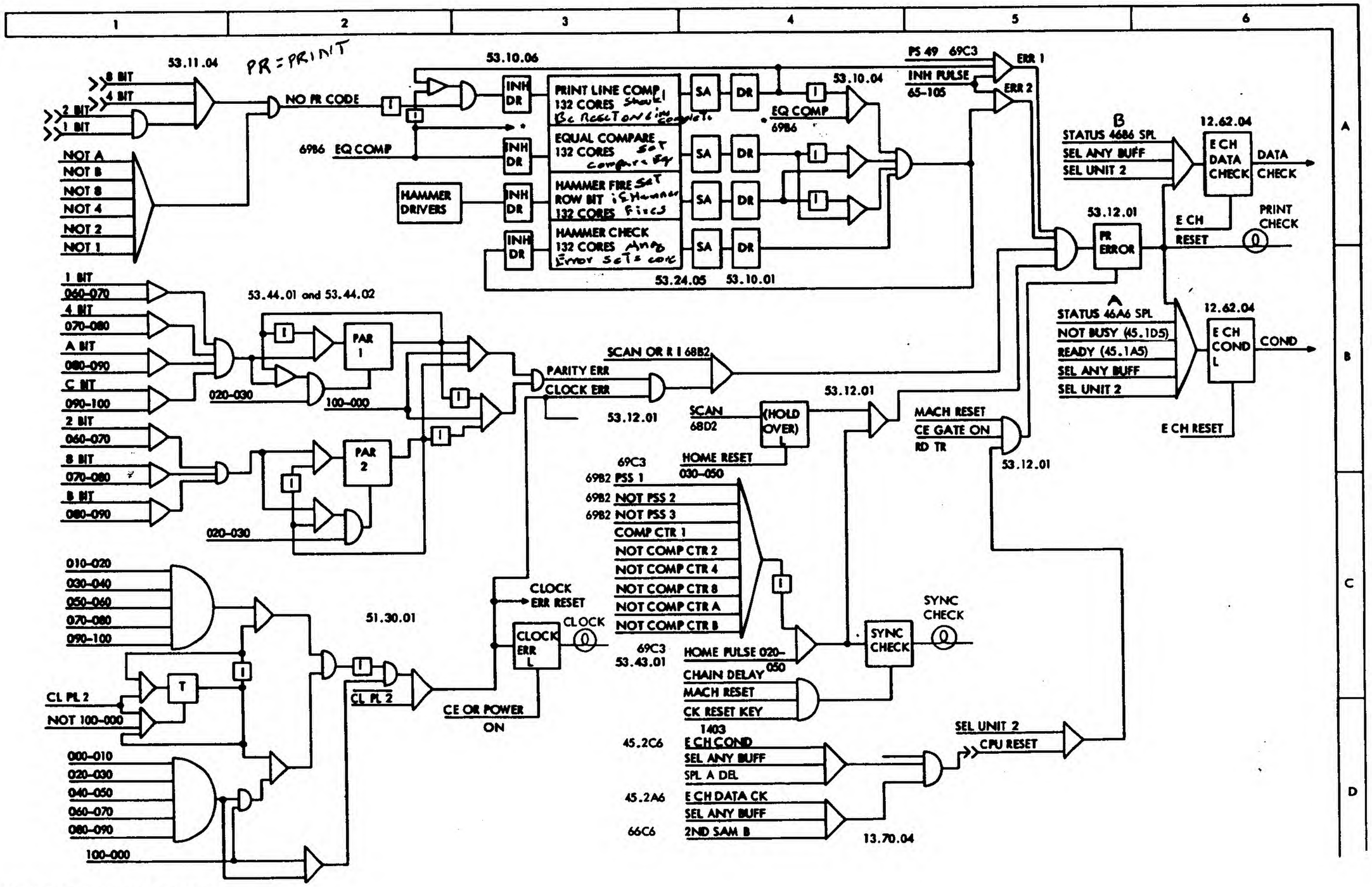


FIGURE 70. PRINT ERROR CIRCUITS

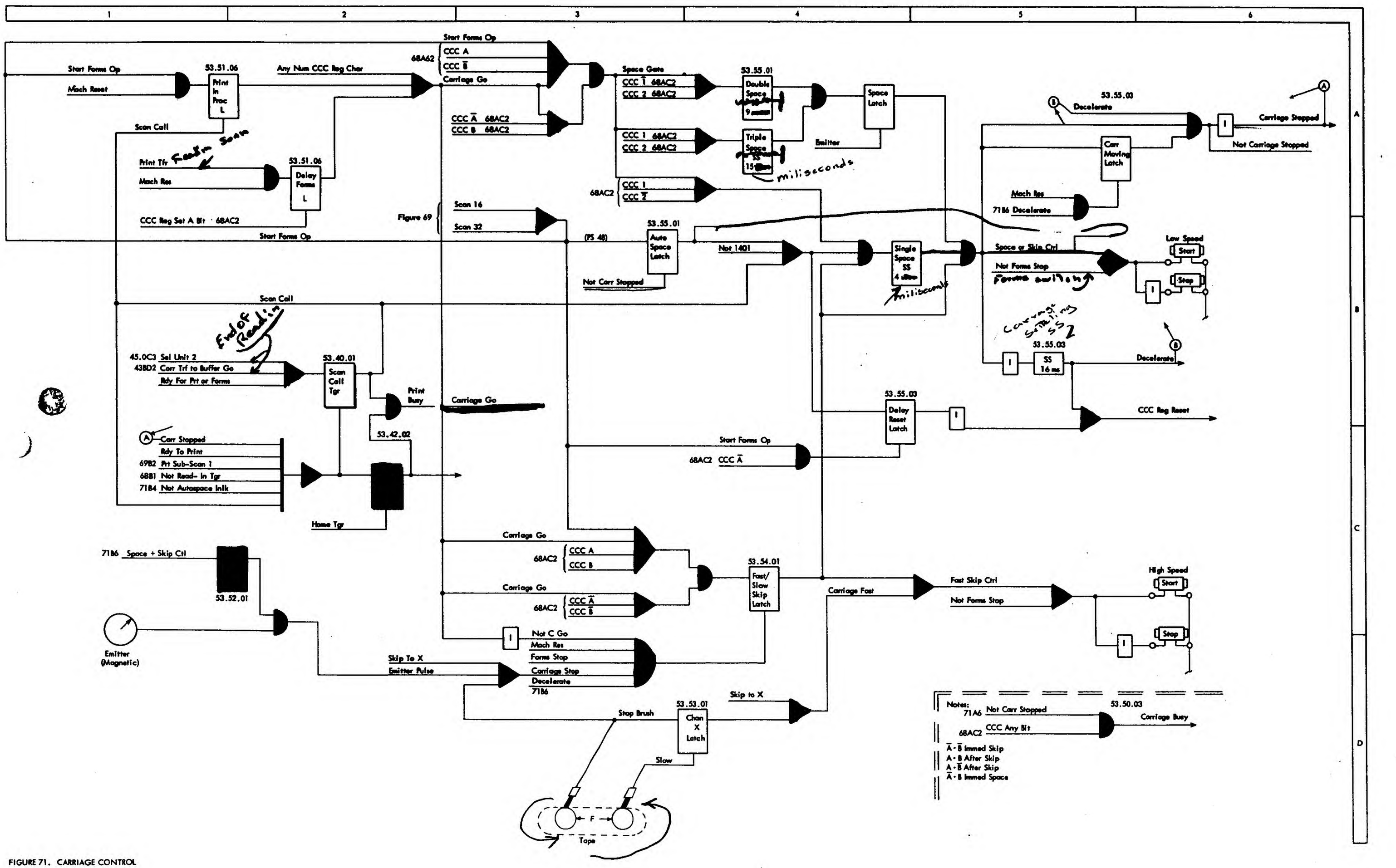


FIGURE 71. CARRIAGE CONTROL

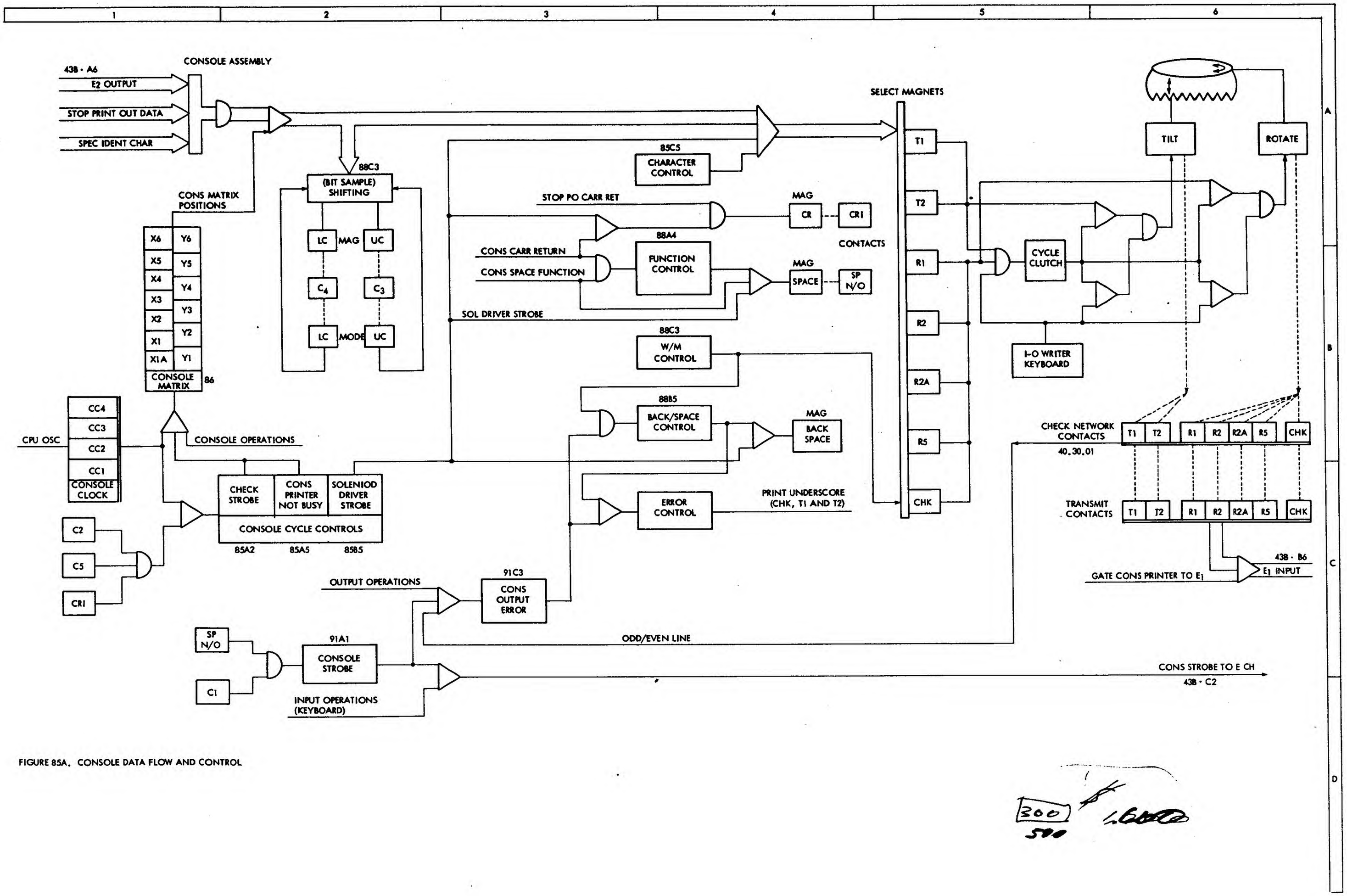
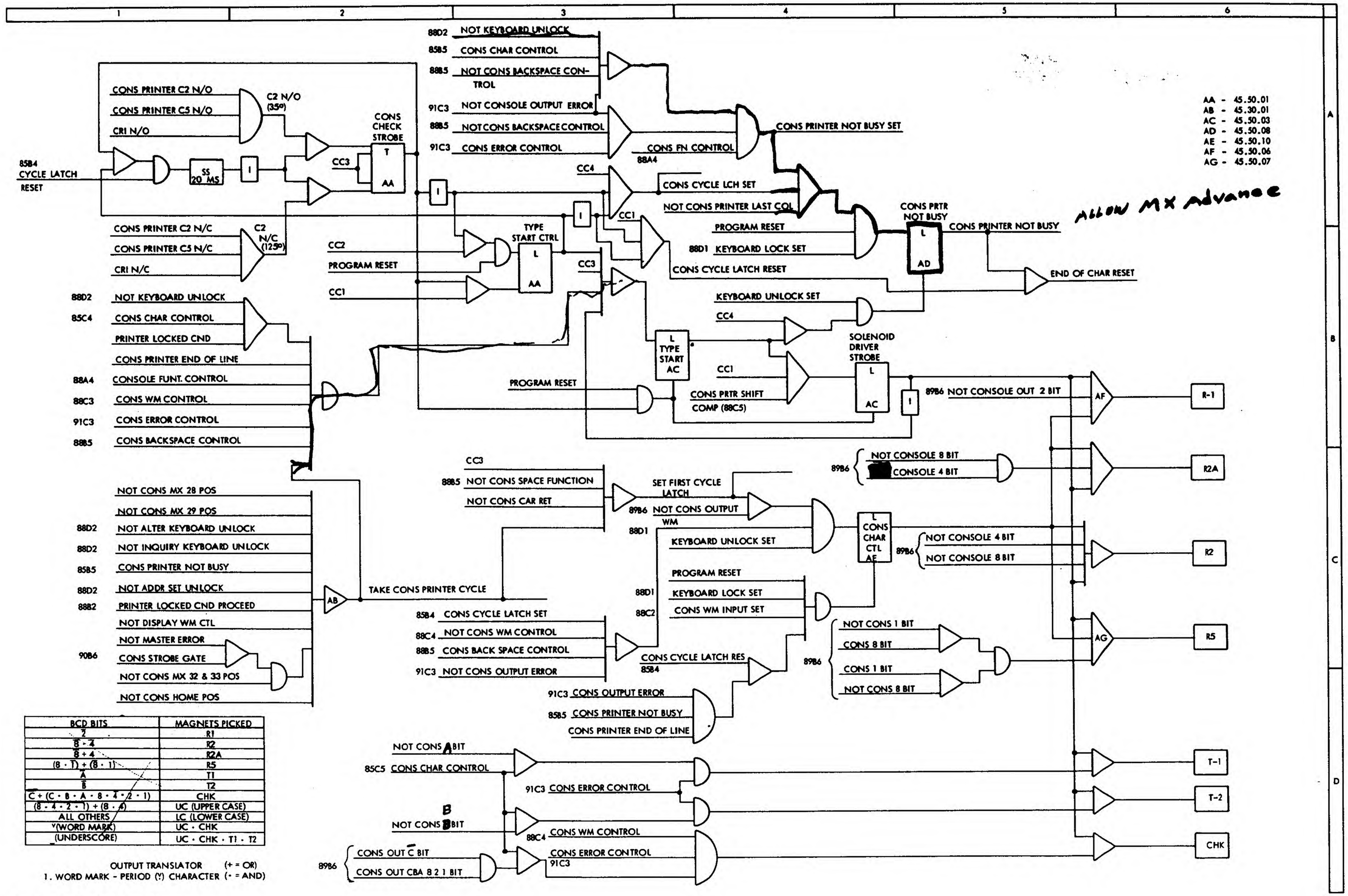


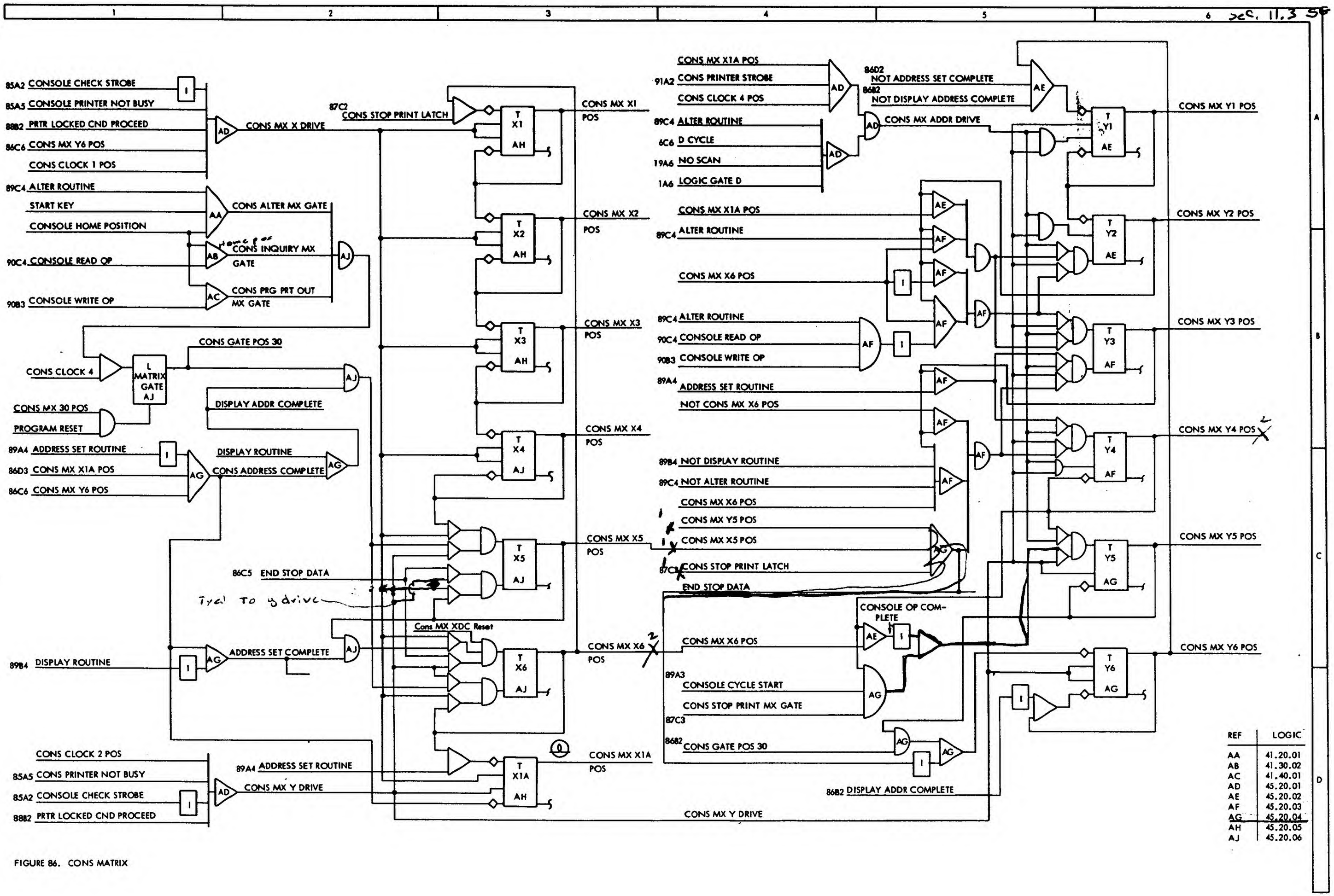
FIGURE 85A. CONSOLE DATA FLOW AND CONTROL



BCD BITS	MAGNETS PICKED
2	R1
B · 4	R2
B + 4	R2A
(8 · 1) + (B · 1)	R5
A	T1
B	T2
C + (C · B · A · 8 · 4 · 2 · 1)	CHK
(8 · 4 · 2 · 1) + (B · A)	UC (UPPER CASE)
ALL OTHERS	LC (LOWER CASE)
˅(WORD MARK)	UC · CHK
(UNDERSCORE)	UC · CHK · T1 · T2

OUTPUT TRANSLATOR (+ = OR)
1. WORD MARK - PERIOD (˅) CHARACTER (· = AND)

FIGURE 85. CONSOLE CONTROL



REF	LOGIC
AA	41.20.01
AB	41.30.02
AC	41.40.01
AD	45.20.01
AE	45.20.02
AF	45.20.03
AG	45.20.04
AH	45.20.05
AJ	45.20.06

FIGURE 86. CONS MATRIX

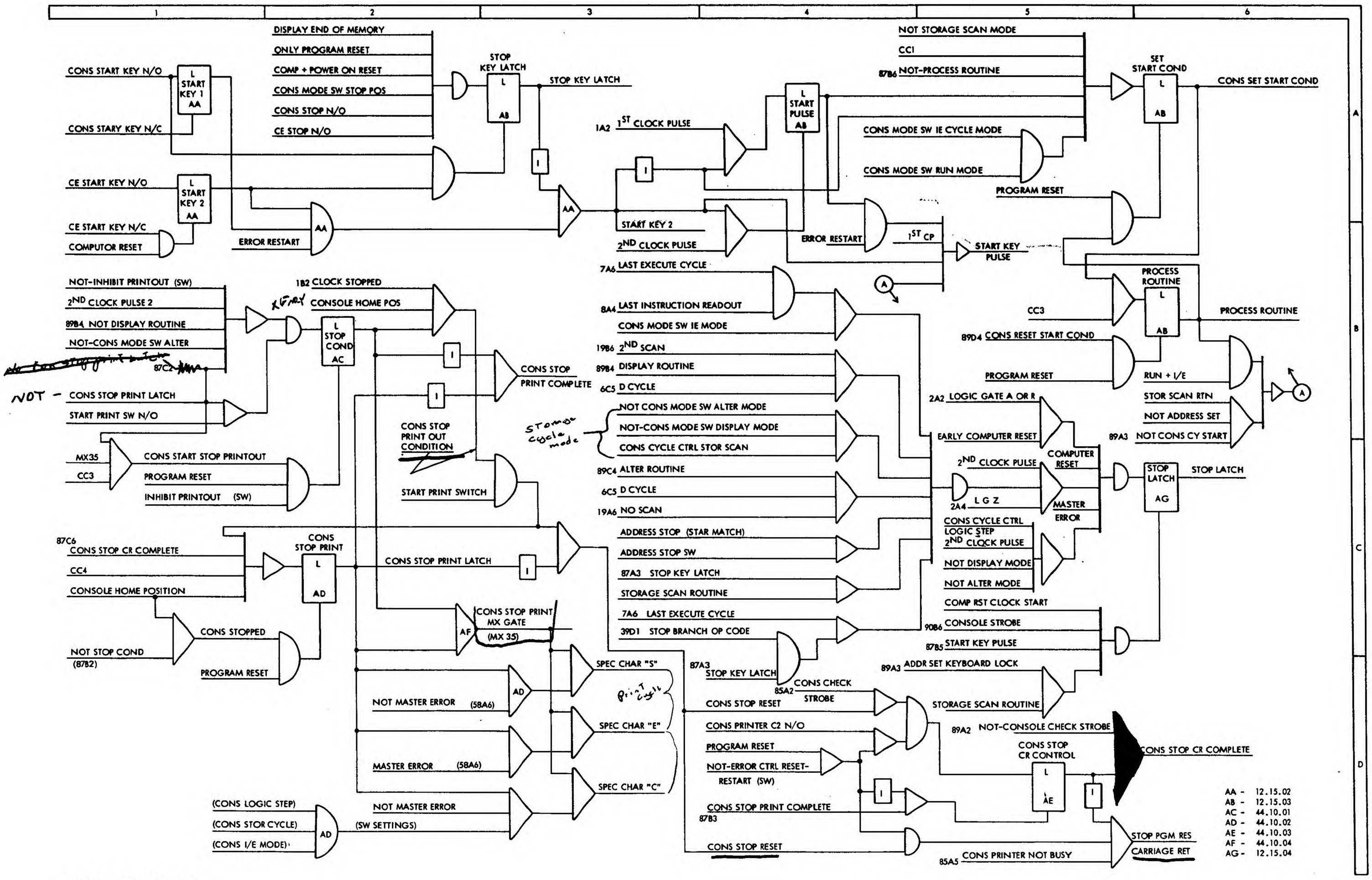


FIGURE 87. CONS START-STOP

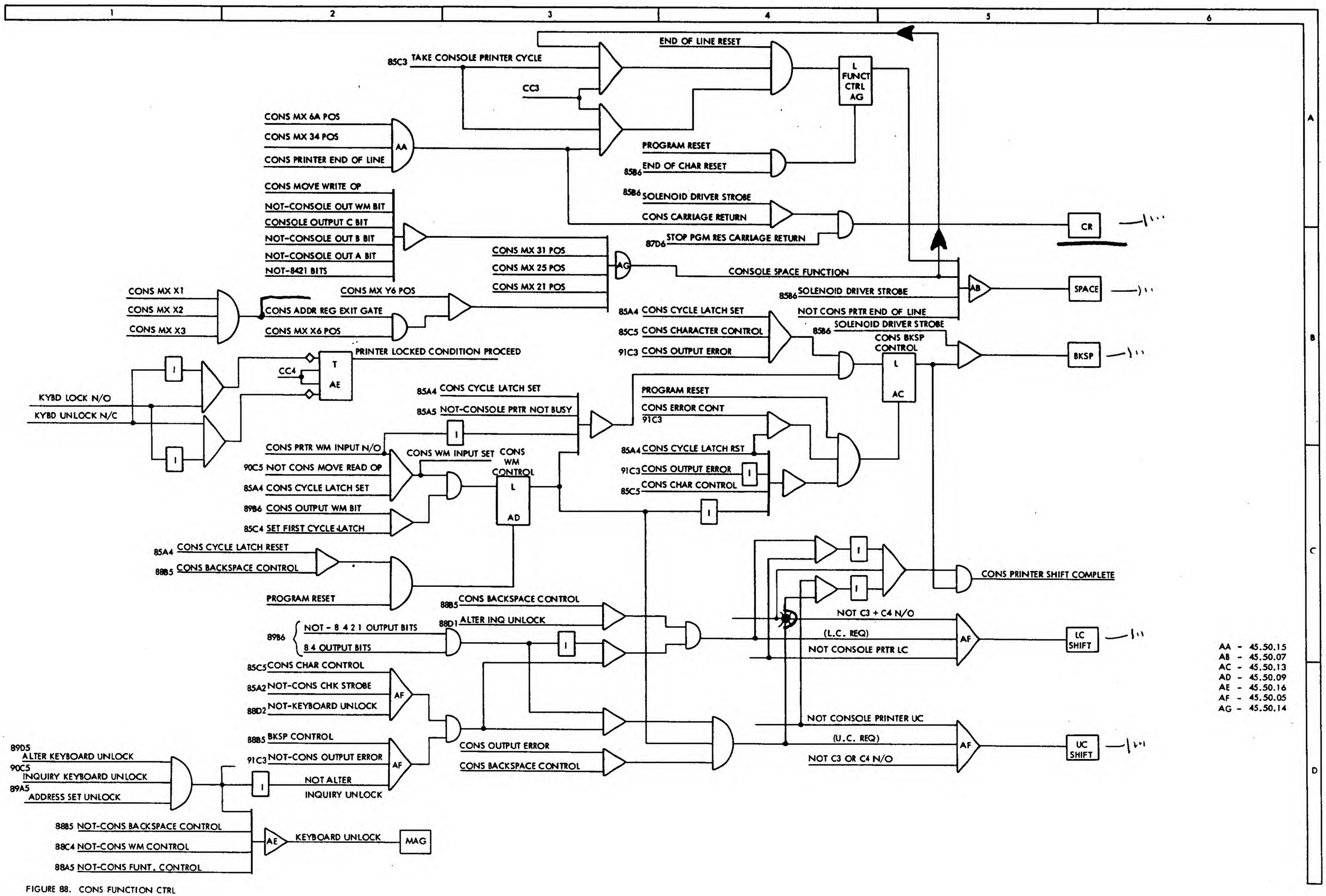
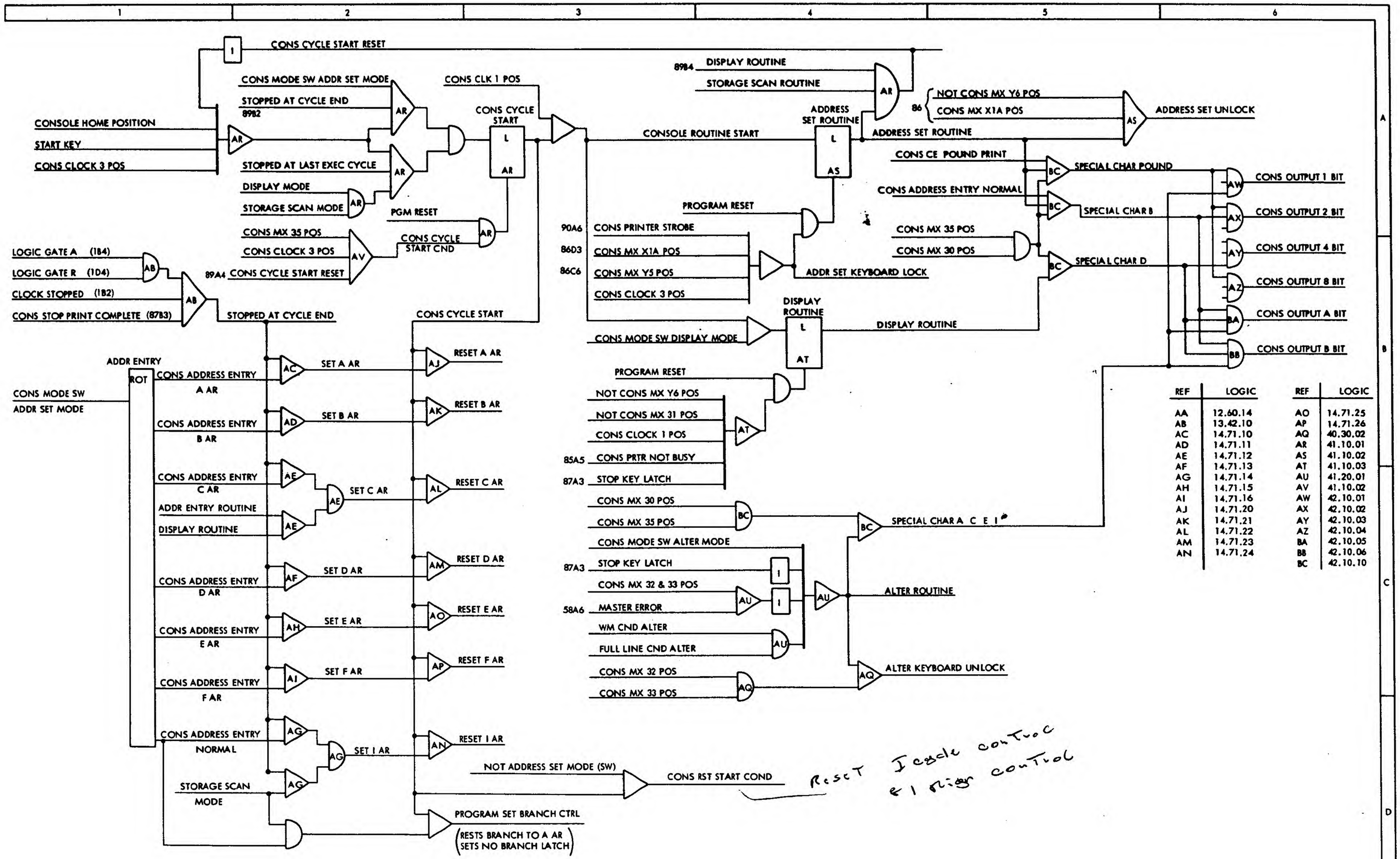
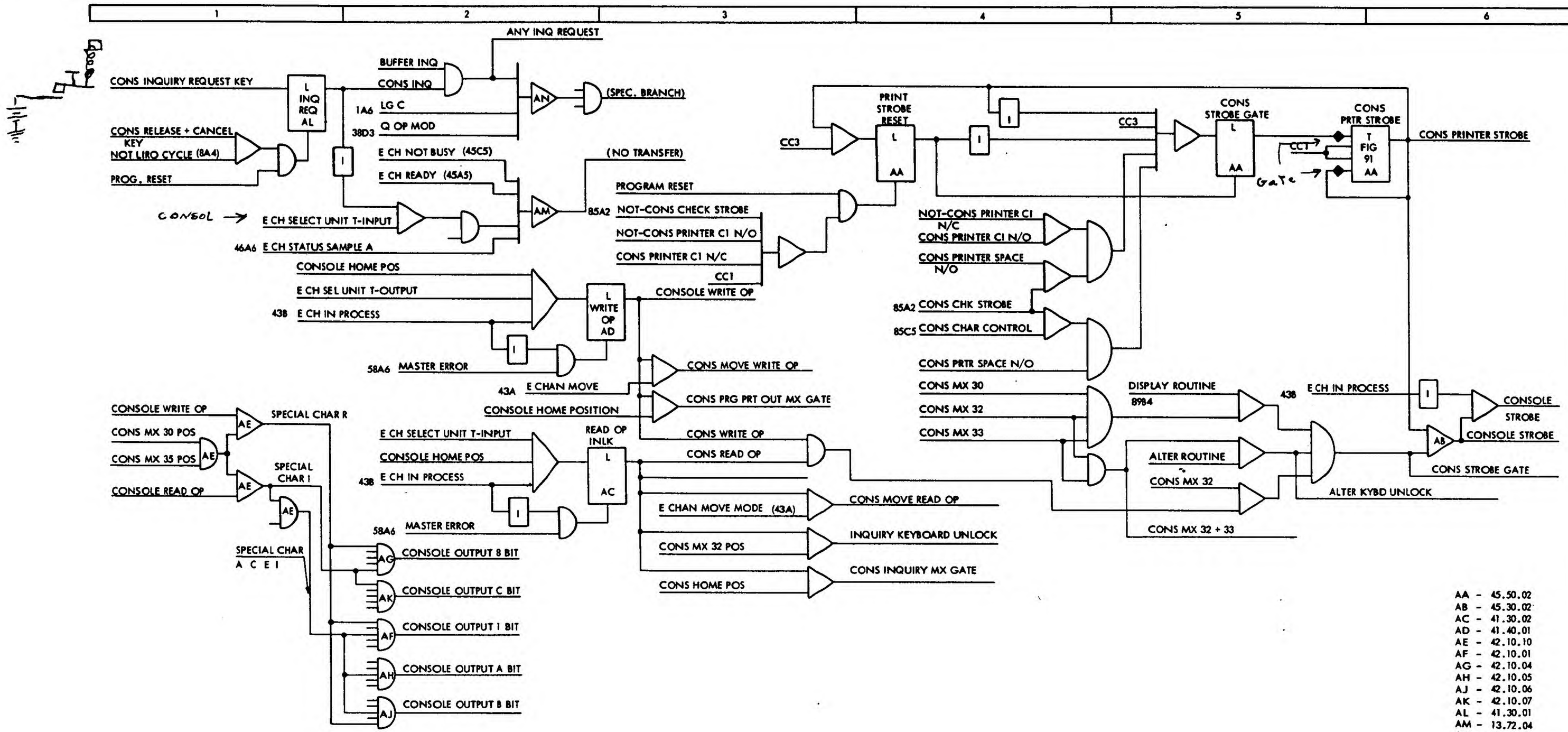


FIGURE 88. CONS FUNCTION CTRL



REF	LOGIC	REF	LOGIC
AA	12.60.14	AO	14.71.25
AB	13.42.10	AP	14.71.26
AC	14.71.10	AQ	40.30.02
AD	14.71.11	AR	41.10.01
AE	14.71.12	AS	41.10.02
AF	14.71.13	AT	41.10.03
AG	14.71.14	AU	41.20.01
AH	14.71.15	AV	41.10.02
AI	14.71.16	AW	42.10.01
AJ	14.71.20	AX	42.10.02
AK	14.71.21	AY	42.10.03
AL	14.71.22	AZ	42.10.04
AM	14.71.23	BA	42.10.05
AN	14.71.24	BB	42.10.06
		BC	42.10.10

FIGURE 89. CONS - START, ADDR SET, DISP, ALT



AA - 45.50.02
AB - 45.30.02
AC - 41.30.02
AD - 41.40.01
AE - 42.10.10
AF - 42.10.01
AG - 42.10.04
AH - 42.10.05
AJ - 42.10.06
AK - 42.10.07
AL - 41.30.01
AM - 13.72.04
AN - 12.61.13

FIGURE 90. CONS RD-WR OP

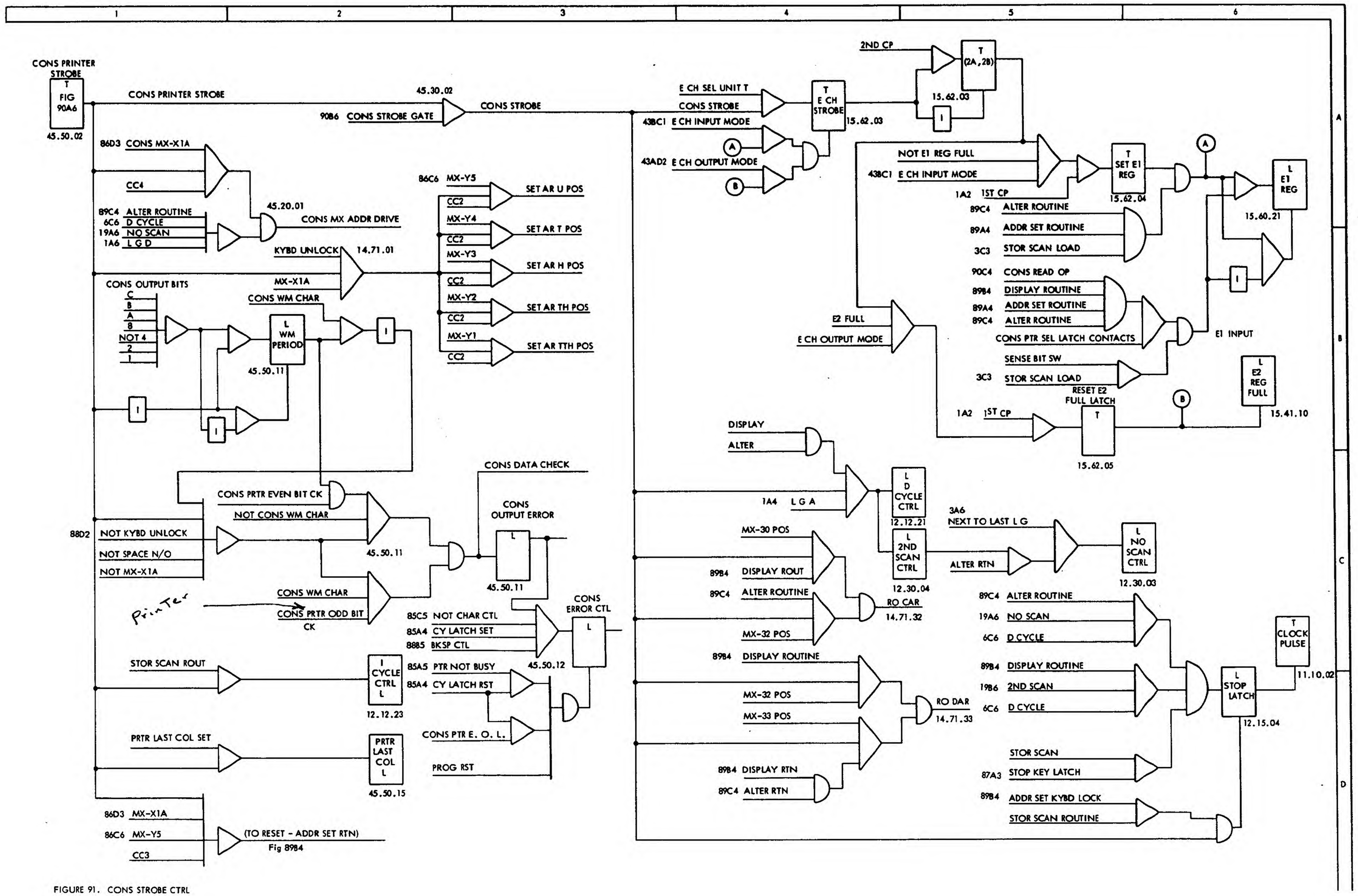


FIGURE 91. CONS STROBE CTRL

INPUTS FROM 729 TAPE DRIVE

02.20.0

729 TP DRV LOGIC		TAPE SYNC ILD
01.03.1	8VPP READ BUS 1 BIT 729	190B1
01.03.1	8VPP READ BUS 2 BIT 729	190B1
01.03.1	8VPP READ BUS 4 BIT 729	190B1
01.03.1	8VPP READ BUS 8 BIT 729	190B1
01.03.1	8VPP READ BUS A BIT 729	190B1
01.03.1	8VPP READ BUS B BIT 729	190B1
01.03.1	8VPP READ BUS C BIT 729	190B1
01.02.1	SEL + RDY WR 729	189A4
01.02.1	SEL + RDY RD 729	189A3
01.09.1	SEL + REWIND 729	185A2
01.05.1	SEL + TI ON 729	183A2
01.02.2	HIGH DENSITY 729	189A1
01.04.1	WRITE ECHO 729	191A1
01.06.1	SEL + LP 729	185A4
01.06.1	SEL + NOT LP 729	189C4
01.05.1	SEL + TI OFF 729	189C4
01.01.1	SEL AND READY MOD 2 729	189A3
01.01.1	SEL AND READY MOD 4 729	189A2
	MOD 5 OR MOD 6	189A2

OUTPUTS TO 729 TAPE DRIVE

02.25.0

TAPE SYNC ILD		729 TP DRV LOGIC
190A4	WRITE BUS 1 BIT 729	01.04.1
190A4	WRITE BUS 2 BIT 729	01.04.1
190A4	WRITE BUS 4 BIT 729	01.04.1
190A4	WRITE BUS 8 BIT 729	01.04.1
190A4	WRITE BUS A BIT 729	01.04.1
190A4	WRITE BUS B BIT 729	
190A4	WRITE BUS C BIT 729	01.04.1
182D2	WRITE PULSE 729	01.04.1
182D6	WR TR REL 729	01.04.1
181C5	SET WR STATUS 729	01.02.1
183C6	SET READ STATUS 729	01.02.1
185C5	BACKWARD 729	01.07.1
189C6	GO 729	01.07.1
185B2	REWIND 729	01.09.1
185D2	REWIND UNLOAD 729	01.09.1
189D3	TURN OFF TI 729	01.05.1
183D2	TURN ON TI 729	01.05.1

INPUTS FROM 7330 TAPE DRIVE

02.21.1

7330 TP DRV LOGIC		TAPE SYNC ILD
73.00.30.0	8VPP READ BUS 1 BIT 7330	190B1
73.00.30.0	8VPP READ BUS 2 BIT 7330	190B1
73.00.30.0	8VPP READ BUS 4 BIT 7330	190B1
73.00.30.0	8VPP READ BUS 8 BIT 7330	190B1
73.00.30.0	8VPP READ BUS A BIT 7330	190B1
73.00.30.0	8VPP READ BUS B BIT 7330	190B1
73.00.30.0	8VPP READ BUS C BIT 7330	190B1
73.00.30.0	SEL + RDY WR 7330	189A4
73.00.30.0	SEL + RDY RD 7330	189A3
73.00.30.0	SEL + REWIND 7330	185A1
73.00.30.0	SEL + TI ON 7330	183A1
73.00.30.0	SEL + RDY HI 7330	189A2
73.00.30.0	ECHO PULSE 7330	191A1
73.00.30.0	SEL + LP 7330	185A4
73.00.30.0	SEL + RDY LO 7330	189A2
73.00.30.0	SEL RDY BWKD 7330	185C3

OUTPUTS TO 7330 TAPE DRIVE

02.26.0

TAPE SYNC ILD		7330 TP DRV LOGIC
190B1	WRITE BUS 1 BIT 7330	73.00.20.0
190B1	WRITE BUS 2 BIT 7330	73.00.20.0
190B1	WRITE BUS 4 BIT 7330	73.00.20.0
190B1	WRITE BUS 8 BIT 7330	73.00.20.0
190B1	WRITE BUS A BIT 7330	73.00.20.0
190B1	WRITE BUS B BIT 7330	73.00.20.0
190B1	WRITE BUS C BIT 7330	73.00.20.0
182D2	WRITE PULSE 7330	73.00.20.0
182D5	WR TR REL 7330	73.00.20.0
181C5	SET WRITE STATUS 7330	73.00.20.0
183C6	SET READ STATUS 7330	73.00.20.0
185C5	BACKWARD 7330	73.00.20.0
189C6	GO 7330	73.00.20.0
185B2	REWIND 7330	73.00.20.0
185D2	REWIND UNLOAD 7330	73.00.20.0
189D3	TURN OFF TI 7330	73.00.20.0
183D2	TURN ON TI 7330	73.00.20.0

INPUTS TO TAPE SYNC

02.30.0

	TAPE SYNC ILD
1 BIT WRITE DATA LINE	190A4
2 BIT WRITE DATA LINE	190A4
4 BIT WRITE DATA LINE	190A4
8 BIT WRITE DATA LINE	190A4
A BIT WRITE DATA LINE	190A4
B BIT WRITE DATA LINE	190A4
C BIT WRITE DATA LINE	190A4
WR CALL	181A5
WR TM CALL	181A6
DISC CALL	182A5
READ CALL	183A6
REWIND CALL	185A2
REWIND + UNLOAD CALL	185B2
BACKSPACE CALL	185A6
ERASE CALL	185A5
TAU RESET	186A1
ODD REDUNDANCY CALL	183A3
TURN OFF TI	189C3
MAN WR DISC	182A5
MANUAL STOP ON ERROR	192B5
MANUAL STOP ON ERROR	192C2
EARLY SAMPLE	192A3
EARLY SAMPLE	191C4
AMPLIFIER BIAS	190A1
COMPARE CHECK CE	192B5
REG A ONLY	191B6
REG B ONLY	191B6
NOT MANUAL OP	181A5
MANUAL ERROR RESET	192A2

OUTPUTS TO CONTROL UNIT

02.35.0

TAPE SYNC ILD	
190A6	R-W REG 1 BIT
190A6	R-W REG 2 BIT
190A6	R-W REG 4 BIT
190A6	R-W REG 8 BIT
190A6	R-W REG A BIT
190A6	R-W REG B BIT
190A6	R-W REG C BIT
181B5	WRITE
182C6	WRITE COND
181D5	BUSY
185B4	LOAD POINT
188B2	CHECK CHAR
183B1	SEL + TI ON
192C2	ERROR
19202	STOP ON ERROR
182D3	WC 2
182C2	WC 8 TR
184B4	WR RC-5 OR READ RC-7
182C2	WC-4
184D5	RC-3
181C3	WD 320 OR WD 1088
188C6	RDD
181C4	WD 49
185B2	SEL + REWIND
189D4	SEL + NOT LP
189D4	SEL + TI OFF
189C2	SEL + READY MOD 4
189B2	SEL + RDY HI 7330
188B5	RDD-36
188B4	RDD 144
188B1	COMPUTE
185C5	BACKWARD

FIGURE 180. TAU INDEX

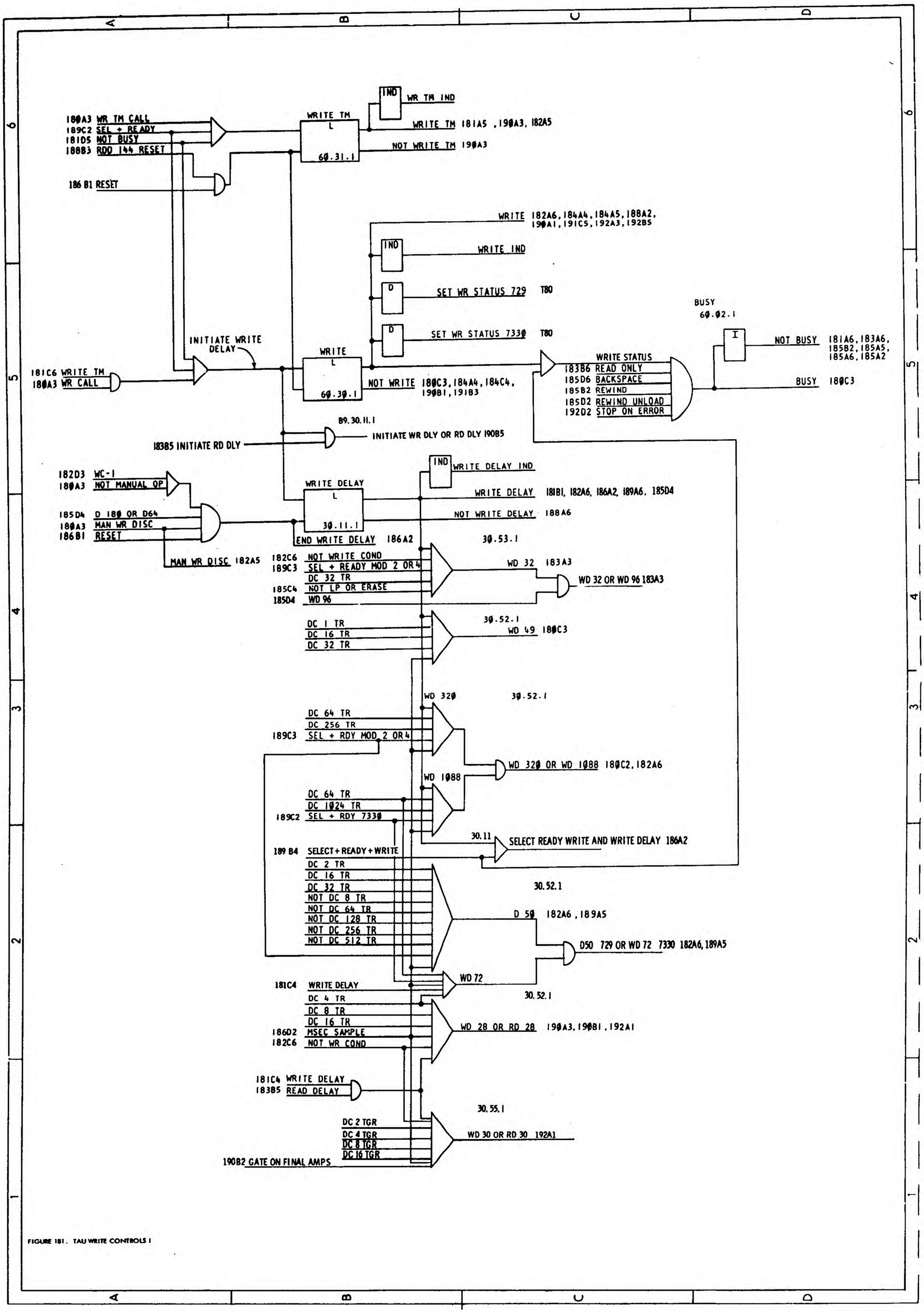


FIGURE 181. TAU WRITE CONTROLS I

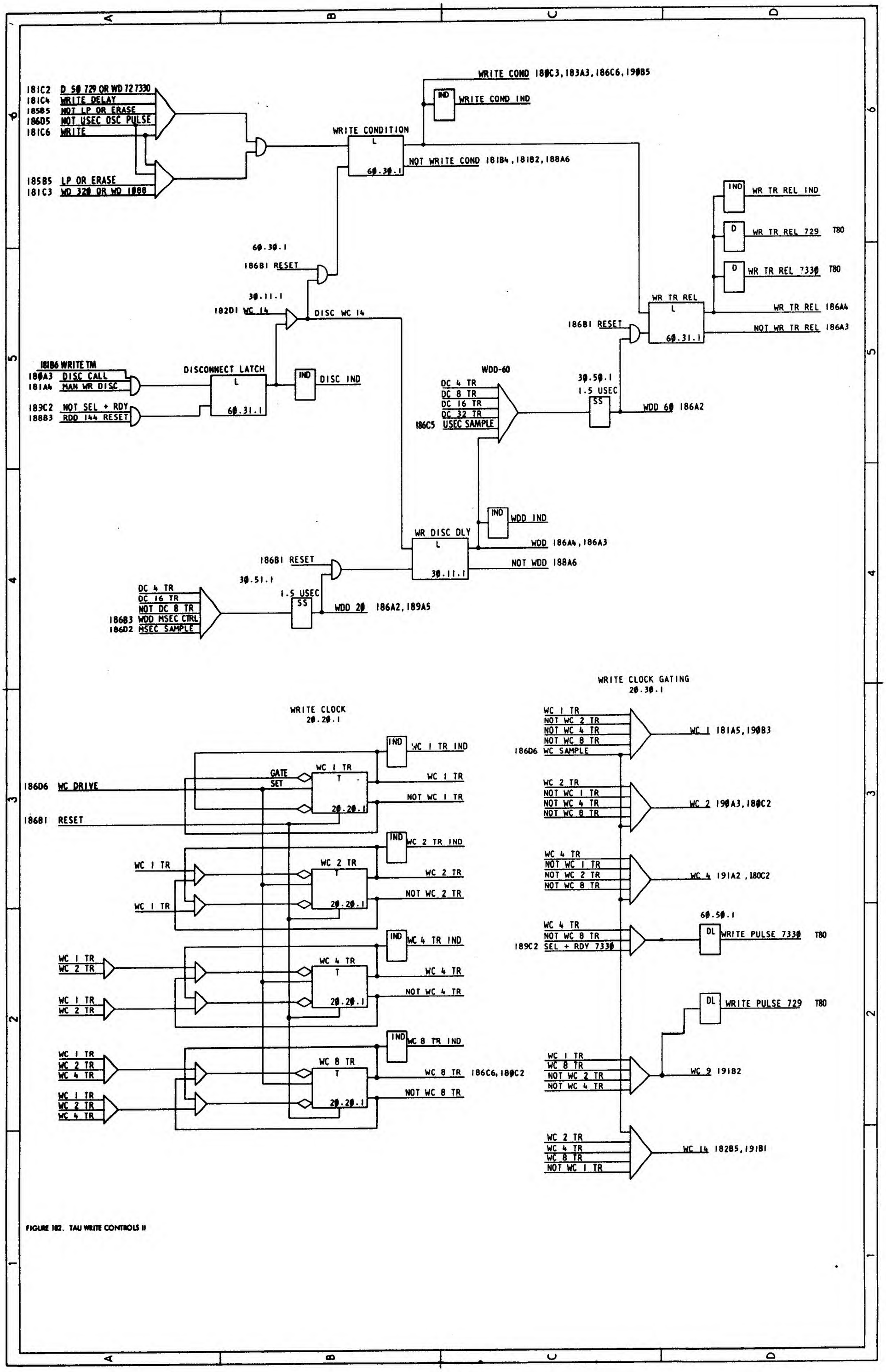


FIGURE 182. TAU WRITE CONTROLS II

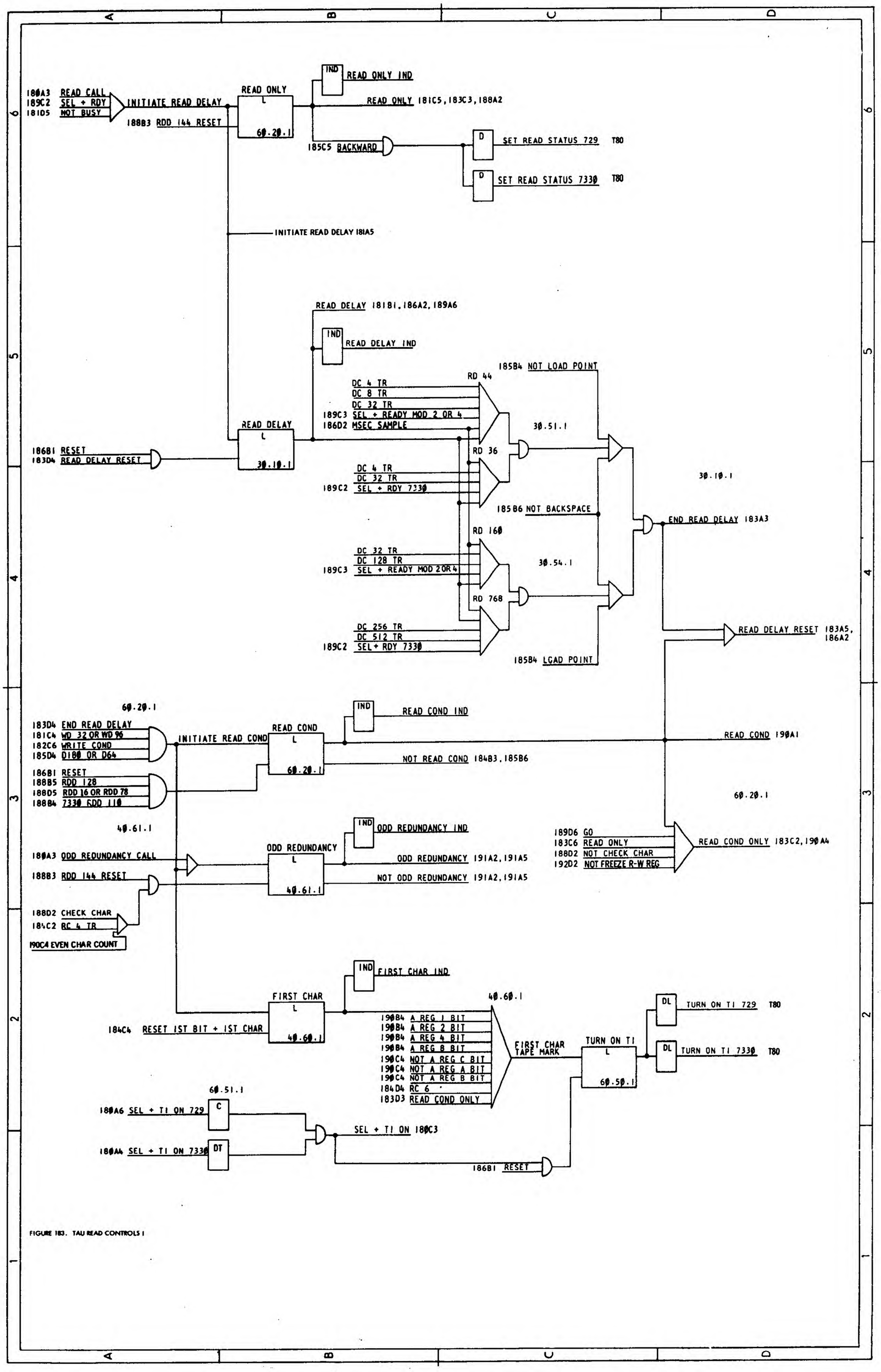


FIGURE 183. TAU READ CONTROLS I

READ RECOGNITION
40.60.1

HI CLIP OUTPUT
190C3
HI CHAN 1 BIT
HI CHAN 2 BIT
HI CHAN 4 BIT
HI CHAN 8 BIT
HI CHAN A BIT
HI CHAN B BIT
HI CHAN C BIT

HI CLIP PULSE 192B4

LO CLIP OUTPUT
190B3
LO CHAN 1 BIT
LO CHAN 2 BIT
LO CHAN 4 BIT
LO CHAN 8 BIT
LO CHAN A BIT
LO CHAN B BIT
LO CHAN C BIT

181C6 WRITE

READ CLOCK OSCILLATOR GATING
10.10.1

IND FIRST BIT IND

1 MC OSC
GATE IN 1MC RD. OSC

360 KC OSC
189C2 SEL + RDY MOD 4
189D1 NOT HIGH DENSITY 729

FIRST BIT L 40.60.1

667 KC OSC
GATE IN 667 KC RD OSC

240 KC OSC
DENSITY 200 SEL
RDY MOD 2 OR 5

320 KC OSC
189D1 SEL + RDY HI 7330

115 KC OSC
189C2 SEL + RDY LO 7330

FIRST BIT 190D3

I READ CLOCK RESET 184B2

READ CLOCK SAMPLE 184A4

I READ CLOCK DRIVE 184B3

READ CLOCK GATING
10.30.1

RC 1 TR
RC 2 TR
NOT RC 4 TR
NOT RC 8 TR
RC 3 191B2 180C2

RC 4 TR
NOT RC 1 TR
NOT RC 2 TR
NOT RC 8 TR
RC 4 188A6, 192A3

RC 2 TR
RC 4 TR
NOT RC 1 TR
181B5 NOT WRITE
RC 6 183B2, 190B3, 192A3

180C6 BACKWARD AT LOAD POINT I

READ CLOCK GATING
10.31.1

181C6 WRITE
RC 2 TR
181C4 NOT WRITE
NOT RC 2 TR
RC 1 TR
RC 4 TR
WR RC-5 OR READ RC-7 188A6, 190C4, 191B5, 192B5, 192B4

READ ONLY

RC 2 TR
RC 8 TR
NOT RC 1 TR
184D5 READ CLOCK SAMPLE
WRITE

WR RC 10 OR READ RC 7 192B5

0.4 USEC
I SS

186B1 RESET
RESET 1ST BIT + 1ST CHAR. 183A2, 192B3

192D2 NOT STOP ON ERROR
183C3 NOT READ COND
WR RC-10 OR READ RC-7 RESET 190C3

186B1 RESET

READ CLOCK
10.20.1

184D5 READ CLOCK DRIVE
184C5 READ CLOCK RESET

IND RC 1 TR IND
RC 1 TR T 10.20.1
RC 1 TR
NOT RC 1 TR

IND RC 2 TR IND
RC 1 TR
RC 1 TR
RC 2 TR T 10.20.1
RC 2 TR
NOT RC 2 TR

IND RC 4 TR IND
RC 1 TR
RC 2 TR
RC 1 TR
RC 2 TR
RC 4 TR T 10.20.1
RC 4 TR 183A3
NOT RC 4 TR

IND RC 8 TR IND
RC 1 TR
RC 2 TR
RC 4 TR
RC 1 TR
RC 2 TR
RC 4 TR
RC 8 TR T 10.20.1
RC 8 TR
NOT RC 8 TR

FIGURE 184. TAU READ CONTROLS II

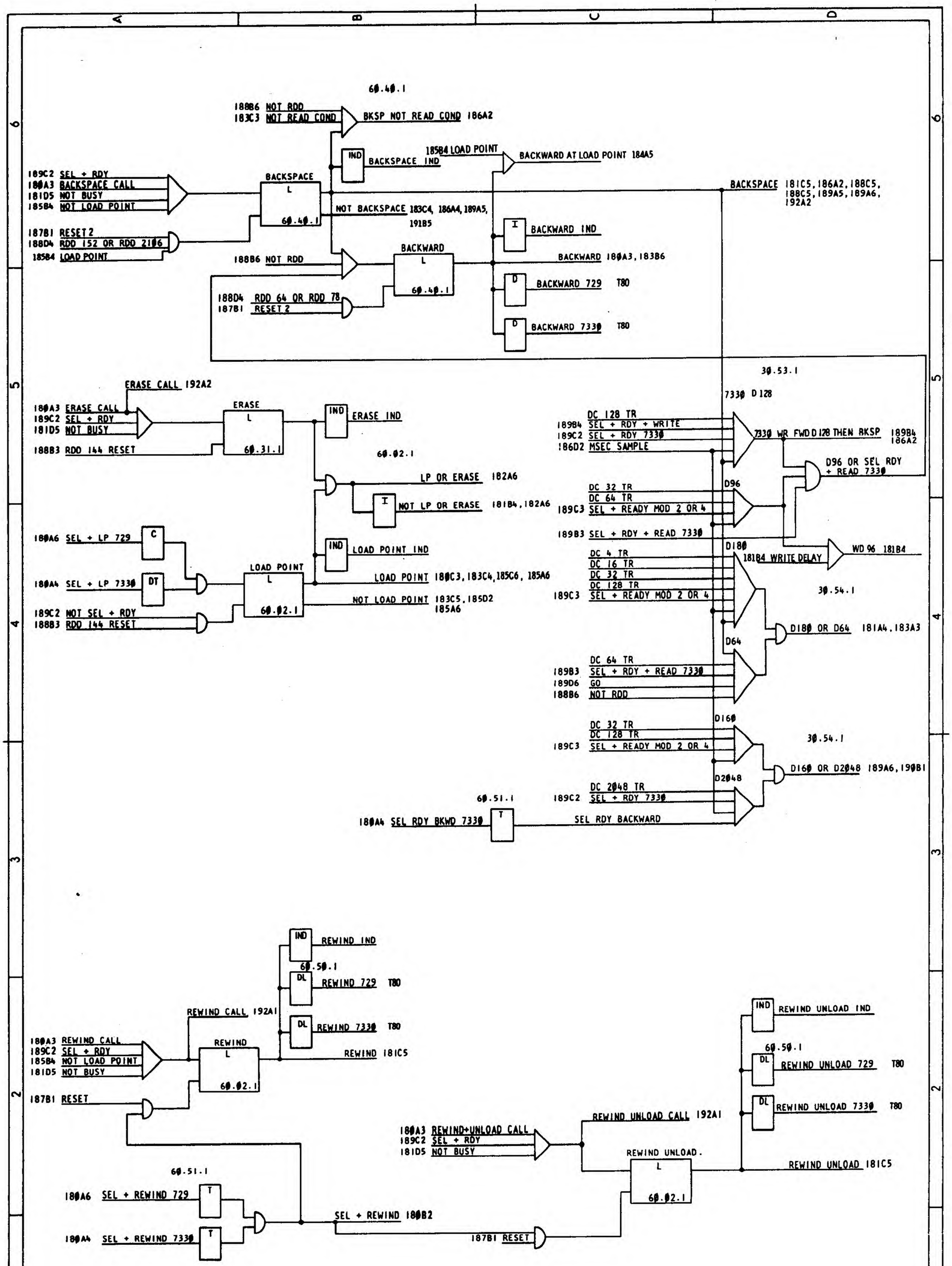


FIGURE 185. TAU UNIT CONTROL

WRITE CLOCK AND DELAY COUNTER OSCILLATOR GATING
20.10.1

960 KC OSC
DENSITY 800 SEL RDY M5

1 MC OSC
189B1 HIGH DENSITY
189C2 SEL + READY MOD 4

360 KC OSC
189B1' NOT HIGH DENSITY
189C2 SEL + READY MOD 4

667 KC OSC
189B2 HIGH DENSITY 729
DENSITY 556
SEL RDY M2+ M5

240 KC OSC
DENSITY 200 SEL RDY M2+ M5

320 KC OSC
189C2 SEL + RDY HI 7330

115 KC OSC
189C2 SEL + RDY LO 7330

182D5 WR TR REL
182C4 WDD
185B6 NOT BACKSPACE
188C6 RDD
USEC CTRL

182C6 WRITE COND
182B2 WC & TR
WC DRIVE 182B3
I
WC SAMPLE 182C3

I
NOT USEC OSC PULSE 182A6

USEC OSC PULSE

30.20.1
USEC SAMPLE 188A5, 182C5

30.20.1
10 KC OSC
189C2 SEL + READY MOD 4
189C2 SEL + RDY 7330
6.7 KC OSC
189C3 SEL + READY MOD 2

30.20.1
DC DRIVE 187B6

182C4 WDD
182D5 NOT WR TR REL
WDD MSEC CTRL 182A4

188C6 RDD
185D6 BACKSPACE
188B3 FWD STOP DELAY
183B5 READ DELAY
185B6 BKSP NOT READ COND
181C2 SELECT READY WRITE AND WRITE DELAY

NOT DC RESET

MSEC SAMPLE 181B2, 182A4, 182C5, 183B5, 185C5, 188C5, 188A2

I

30.31.1
182B4 WDD 20
182C5 WDD 60
183D4 READ DELAY RESET
188B6 END RDD
181B4 END WRITE DELAY
185D5 7330 WR FWD D 128 THEN BKSP
185C6 BACKWARD AT LOAD POINT

1.5 USEC SS
DC RESET 187B6

180A3 TAU RESET
RESET 181, 182, 183, 184, 185, 188, 189, 190, 192

FIGURE 186. TAU WR CLOCK AND DLY CTR OSC GATING

DELAY COUNTER
30.40.1

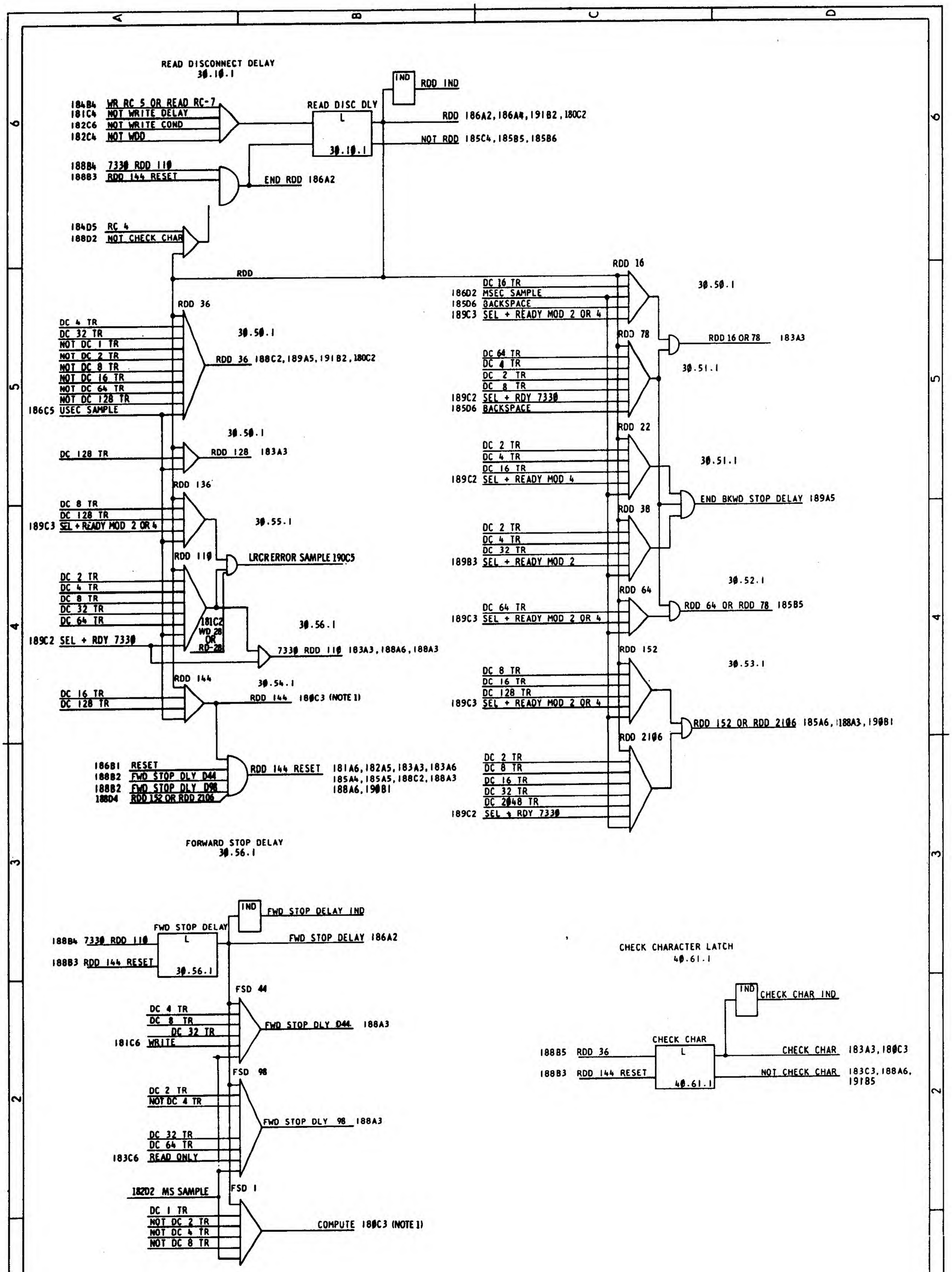
18603 DC DRIVE
18602 DC RESET

DC 1 T 30.40.1 — GATE SET
DC 2 T 30.40.1 — DC 1 TR
DC 4 T 30.40.1 — DC 2 TR
DC 8 T 30.41.1 — DC 4 TR
DC 16 T 30.42.1 — DC 8 TR
DC 32 T 30.42.1 — DC 16 TR
DC 64 T 30.42.1 — DC 32 TR
DC 128 T 30.42.1 — DC 64 TR
DC 256 T 30.43.1 — DC 128 TR
DC 512 T 30.43.1 — DC 256 TR
DC 1024 T 30.43.1 — DC 512 TR
DC 2048 T 30.43.1 — DC 1024 TR

IND — DC 1 TR IND
IND — DC 2 TR IND
IND — DC 4 TR IND
IND — DC 8 TR IND
IND — DC 16 TR IND
IND — DC 32 TR IND
IND — DC 64 TR IND
IND — DC 128 TR IND
IND — DC 256 TR IND
IND — DC 512 TR IND
IND — DC 1024 TR IND
IND — DC 2048 TR IND

NOT DC 1 TR
NOT DC 2 TR
NOT DC 4 TR
NOT DC 8 TR
NOT DC 16 TR
NOT DC 32 TR
NOT DC 64 TR
NOT DC 128 TR
NOT DC 256 TR
NOT DC 512 TR
NOT DC 1024 TR
NOT DC 2048 TR

FIGURE 187. TAU DELAY COUNTER



NOTE 1: RESET THE TAPE IN PROCESS LATCH IN CONTROL UNITS.

FIGURE 180. TAU RDD, FSD AND CHECK CHARACTER

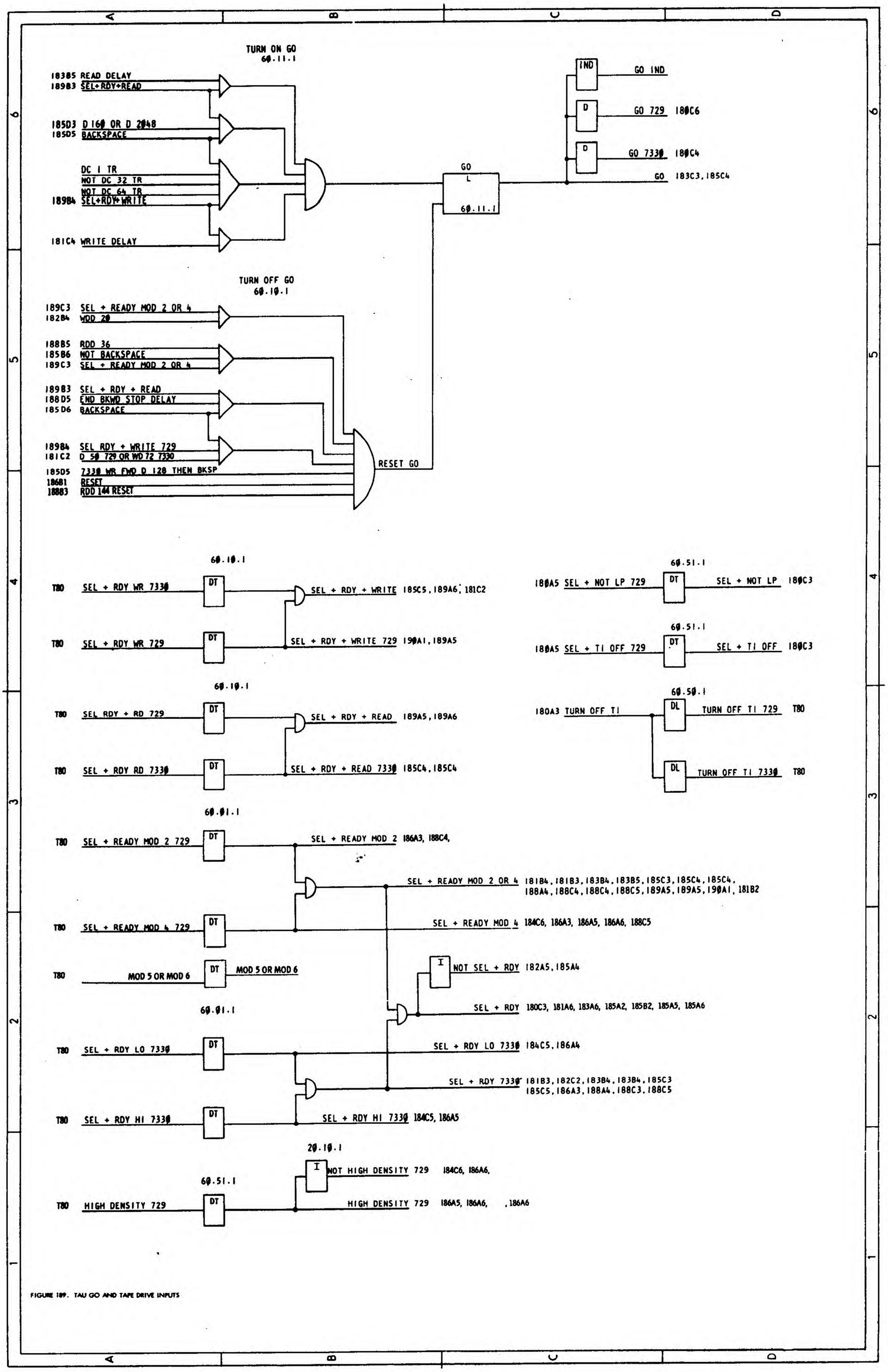


FIGURE 189. TAU GO AND TAPE DRIVE INPUTS

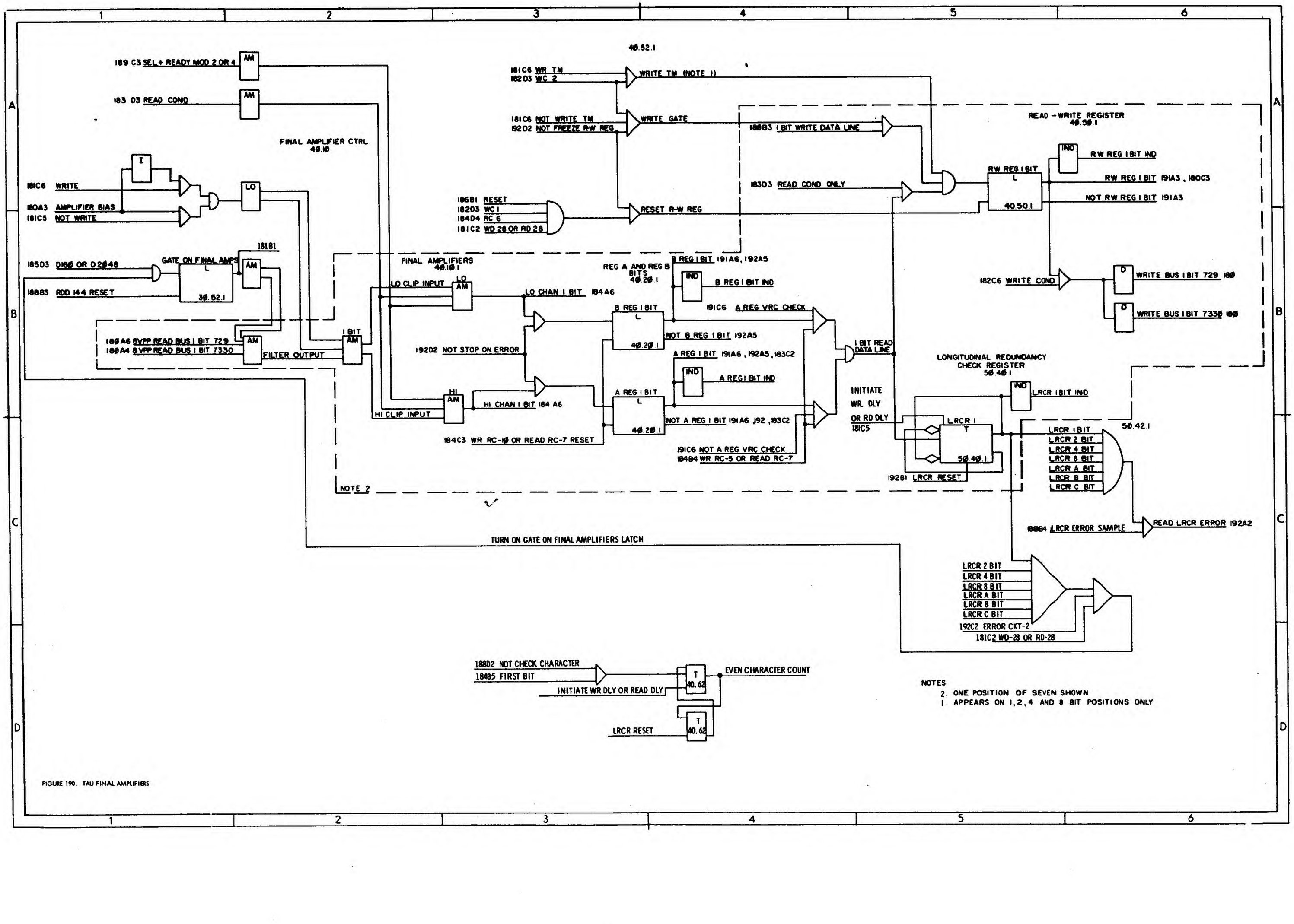


FIGURE 190. TAU FINAL AMPLIFIERS

A REG VRC
50.10.1

A REG 1 BIT
NOT A REG 2 BIT
NOT A REG 1 BIT
A REG 2 BIT
A REG 4 BIT
NOT A REG 8 BIT
NOT A REG 4 BIT
A REG 8 BIT
19084
A REG A BIT
NOT A REG B BIT
NOT A REG A BIT
A REG B BIT
A REG C BIT
183C2 NOT ODD REDUNDANCY
190B4 NOT A REG C BIT
183C2 ODD REDUNDANCY

CE PANEL
180A3 REG A ONLY
180A3 REG B ONLY

A REG VRC CHECK 19084
NOT A REG VRC CHECK 190C4

18484 WR RC-5 OR READ RC-7
18802 NOT CHECK CHAR
18586 NOT BACKSPACE
192B2 ERROR RESET

A REG VRC
L
50.51.1

IND A REG VRC ERROR IND
WR A REG VRC CHECK 192A2
181C6 WRITE
EARLY SAMPLE A REG VRC 192A2
180A2 EARLY SAMPLE (CE)

READ WRITE REG VRC
50.20.1

RW REG 1 BIT
NOT RW REG 2 BIT
NOT RW REG 1 BIT
RW REG 2 BIT
RW REG 4 BIT
NOT RW REG 8 BIT
NOT RW REG 4 BIT
RW REG 8 BIT
190A6
RW REG A BIT
NOT RW REG B BIT
NOT RW REG A BIT
RW REG B BIT
RW REG C BIT
183C3 NOT ODD REDUNDANCY
190A6 NOT RW REG C BIT
183C3 ODD REDUNDANCY

188B5 RDD 36
181B5 NOT WRITE
188B6 RDD
184D5 RC 3
182D2 WC 9

RW REG VRC ERROR 192A2

R-W REG VRC
L
50.50.1

IND RW REG VRC IND
RW REG ERR LATCH 192C2
192B2 ERROR RESET

ECHO ERROR
50.50.1

IND NO ECHO IND
NO ECHO
L
50.50.1
182D3 WC 4
182D1 WC 14

ECHO ERROR 192A2
ECHO ERR
L
50.50.1
192B2 ERROR RESET
IND ECHO ERROR IND

T80 WRITE ECHO 729 C
T80 ECHO PULSE 730 DT
192B2 ERROR RESET

FIGURE 191. TAU ERROR CIRCUITS I

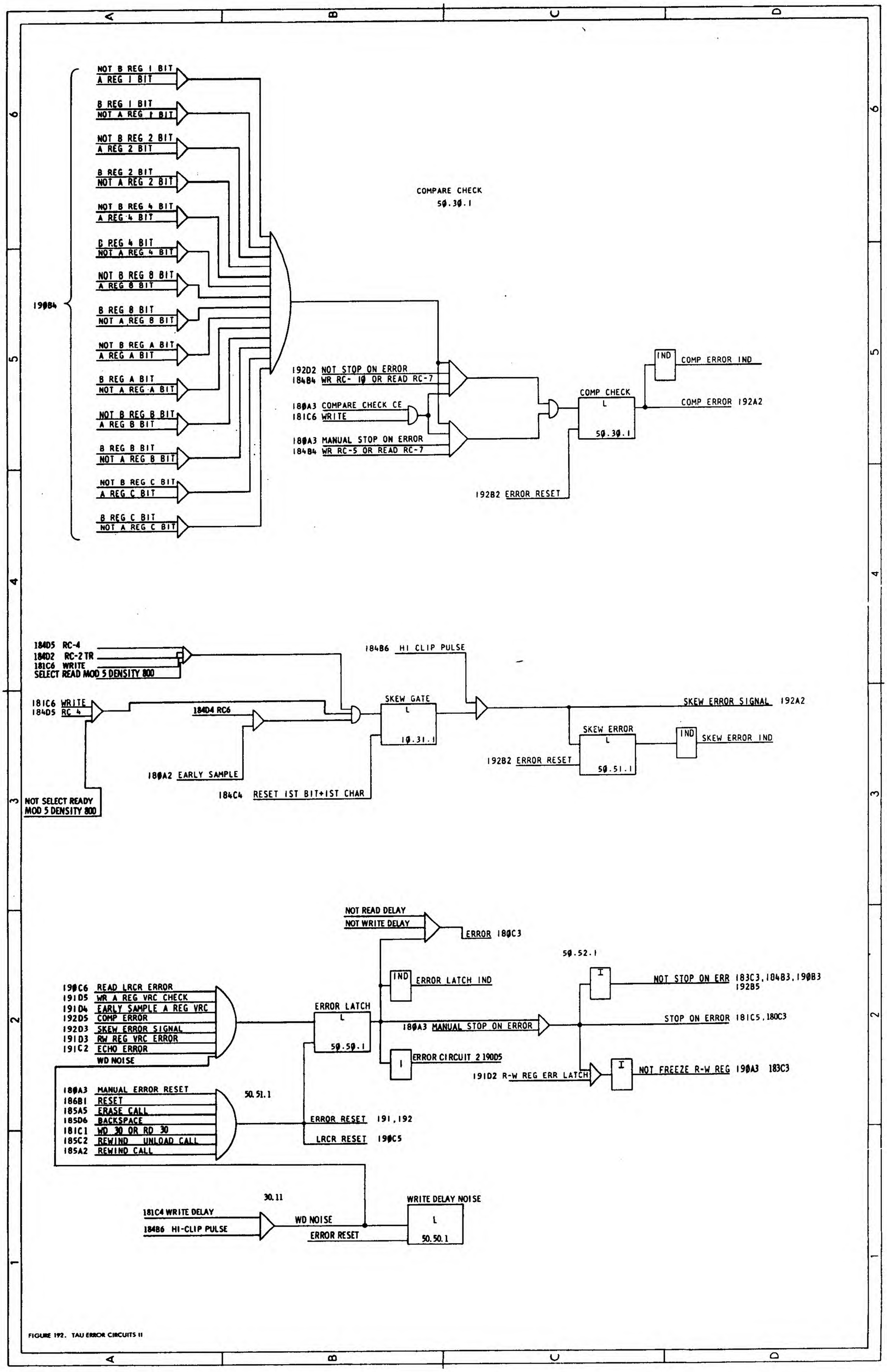


FIGURE 192. TAU ERROR CIRCUITS II

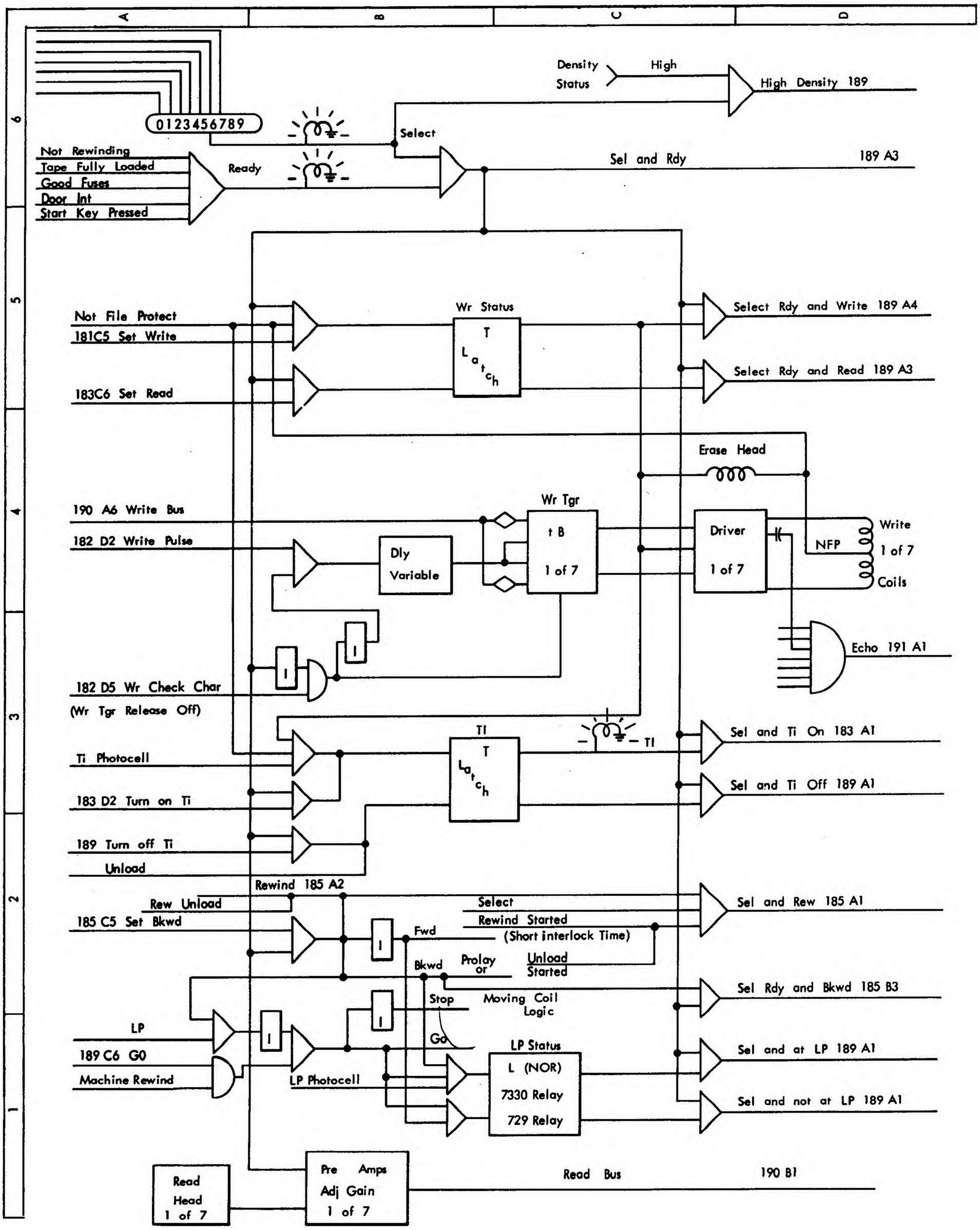


FIGURE T80. TAPE UNIT RESPONSE LOGIC

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